Simulation of twin boundary effect on characteristics of single grain-silicon thin film transistors

F. Yan[a)]
Department of Applied Physics, The Hong Kong Polytechnic University, Hong Kong, China

P. Migliorato
Department of Engineering, Cambridge University, Trumpington Street, Cambridge CB2 1PZ, United Kingdom,

R. Ishihara
Laboratory of Electronic Components, Technology and Materials (ECTM), Delft Institute of Microelectronics and Submicrontechnology (DIMES), Delft University of Technology, Feldmannweg 17, 2600 GB Delft, The Netherlands

(Received 20 May 2007; accepted 18 July 2007; published online 14 August 2007)

The influence of twin boundaries on the characteristics of single grain-silicon thin film transistors has been analyzed by three-dimensional simulation. The simulations show that the orientation and the location of a twin boundary could affect the field-effect mobility and the leakage current of a device. The field-effect mobility increases with the increase of the angle between the normal direction of the twin boundary and the channel direction. A single twin boundary in contact with the drain can lead to higher leakage current because electron-hole generation is greatly enhanced by the trap states in the twin boundary. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2769951]

Thin film transistors have been widely used in flat panel displays. Excimer-laser crystallization of amorphous silicon films is a well-established method for producing large-grain polycrystalline-silicon thin film transistors (poly-Si TFTs) on glass substrates, which makes it possible to achieve the system-on-panel active matrix liquid crystal display.[1] Poly-Si TFTs have much higher field-effect mobility, typically about 100 $cm^2/V\,s$, compared to that of amorphous silicon TFTs. However, it is still much lower than that of metal-oxide-silicon transistors formed on bulk Si wafers. Recently, thanks to a technique referred to as micro-Czochralski or grain-filter process,[2–4] TFTs can be fabricated on a location controlled silicon single grain. Much higher mobilities (400 $cm^2/V\,s$) than that of standard laser-crystallized poly-Si TFT are obtained in such single grain TFT (SG-TFT). However, device to device nonuniformities are sometimes observed and attributed to the presence of twin boundaries,[5,6] which is very similar to the case found in poly-Si devices with big grain size.[7,8] The effect of twin boundaries on the performance of TFT has been well recognized and several one- or two-dimensional analytical models have been developed for studying this effect.[9] However, to characterize the effect of a twin boundary with an arbitrary orientation, three-dimensional (3-D) simulation is an essential technique. In this letter, we will report the 3D simulation of SG-TFTs and investigate the effect of a twin boundary in the devices, including its influence on field-effect mobility and off current.

Integrated systems engineering (ISE) commercial package Version 9.0 has been used for the 3D simulation. The geometry of the device, doping density, and mesh for the simulation are generated by 3D device editor DEVISE and the electric behavior of the device is simulated by DESSIS.

In the simulation, there are three governing equations for charge transport in semiconductor devices that are the Poisson equation and the two electron and hole continuity equations. The Poisson equation is stated as

$$\nabla\varepsilon\cdot\nabla\psi = -q(p-n+N_{D+}-N_{A-}), \tag{1}$$

where N_{D+} and N_{A-} are the number of ionized donors and acceptors, respectively, n and p are the electron and hole density, and ε is the electrical permittivity.

The electron and hole continuity equations are written as follows:

$$\nabla\cdot\vec{J_n} = qR + q\frac{\partial n}{\partial t}, \tag{2}$$

$$\nabla\cdot\vec{J_p} = qR + q\frac{\partial p}{\partial t}, \tag{3}$$

where R is the net electron-hole recombination rate and J_n and J_p are the electron and hole current density.

In high electric field, free carriers gain very high energy. Thus their temperature is not equal to the lattice temperature. In order to account for hot carrier effect, the hydrodynamic model has been adopted in the simulation.[10] In this model, the current densities are defined as follows:

$$\vec{J_n} = \mu_n(n\nabla E_C + kT_n\nabla n + f_n^{td}kn\nabla T_n - 1.5nkT_n\nabla\ \ln m_e), \tag{4}$$

$$\vec{J_p} = \mu_p(p\nabla E_V - kT_p\nabla p - f_p^{td}kp\nabla T_p - 1.5pkT_p\nabla\ \ln m_h), \tag{5}$$

where E_C and E_V are the conduction and valence band energies, respectively, and T_n and T_p are the temperature of electrons and holes, respectively. m_e and m_h are effective masses of electrons and holes. f_n^{td} and f_p^{td} are parameters for electrons and holes.

Figure 1(a) shows a n-channel SG-TFT structure used in the simulation. The thickness of gate oxide is 100 nm and the gate size is $W/L=2\ \mu m/2\ \mu m$. The active thickness of Si film is 250 nm, which is similar to that of the real devices reported before.[4] In the cross-sectional view, as shown in

[a)]Electronic mail: apafyan@polyu.edu.hk

 © 2007 American Institute of Physics
Downloaded 19 Aug 2011 to 158.132.161.52. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

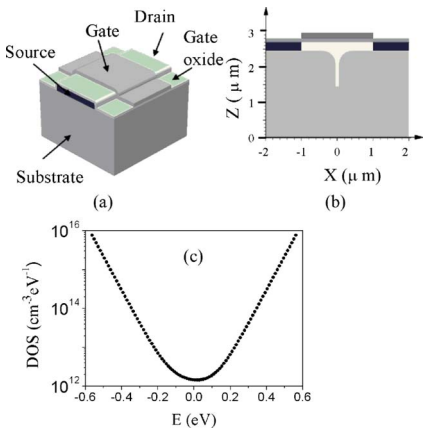

FIG. 1. (a) 3D SG-TFT device generated with DEVISE in ISE. (b) Cross-sectional view of the SG-TFT. (c) Density of trap states assumed in the twin boundary in the simulation.

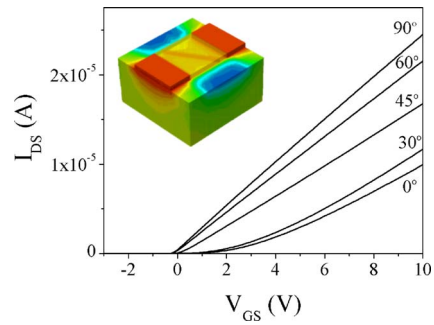

FIG. 2. Transfer characteristics of SG-TFTs with a single twin boundary in the middle of the channel oriented to different directions. $V_{DS}=0.1$ V. From top to bottom, the transfer curves correspond to the angles between the normal directional of the twin boundary and the channel direction, 90°, 60°, 45°, 30°, and 0°, respectively. Inset: A SG-TFT without the metal gate and the gate oxide, in which a twin boundary in the channel has an angle of 30° relative to the channel direction.

Fig. 1(b) a circular hornlike hole named grain filter has a diameter of 100 nm at the bottom. The geometric size of the single grain Si in the device is very similar to the real device reported by Ishihara *et al.*[4] In the simulation, the trap state density and the capture cross section need to be set with reasonable values. We model the twin boundary as a planar defect with a density of gap states.[11] Four exponential distributions of the density of states (DOS) have been used as indicated in the following equation:

$$N(E) = N_{at}e^{(E-E_C)/E_{at}} + N_{ad}e^{(E-E_C)/E_{ad}} + N_{dt}e^{(E_V-E)/E_{dt}} + N_{dd}e^{(E_V-E)/E_{dd}}, \quad (6)$$

where the subscripts a and d refer to acceptorlike and donorlike states, respectively, and the subscripts t and d refer to tail and deep states, respectively. Figure 1(c) shows the DOS in the twin boundary we used for the simulation, which was generated with the data below:

$$N_{at} = 5 \times 10^{15}\text{cm}^{-2}\ \text{eV}^{-1},$$

$$E_{at} = 0.05\ \text{eV},$$

$$N_{ad} = 2 \times 10^{12}\text{cm}^{-2}\ \text{eV}^{-1},$$

$$E_{ad} = 0.33\ \text{eV},$$

$$N_{dt} = 5 \times 10^{15}\text{cm}^{-2}\ \text{eV}^{-1},$$

$$E_{dt} = 0.05\ \text{eV},$$

$$N_{dd} = 4.5 \times 10^{12}\text{cm}^{-2}\ \text{eV}^{-1},$$

$$E_{dd} = 0.33\ \text{eV}. \quad (7)$$

To accurately simulate the off current, the Shorkley-Read-Hall generation-recombination model has been adopted in the simulation. The capture cross sections of trap states are assumed to be $\sigma_{nd}=10^{-13}$ cm^2, $\sigma_{na}=10^{-15}$ cm^2, $\sigma_{pd}=10^{-15}$ cm^2, and $\sigma_{pa}=10^{-13}$ cm^2. $\sigma_{n(p)d(a)}$ is the electron (hole) capture cross section of donor (acceptor) states.

It has been reported that the orientation of twin boundary had pronounced influence on the field-effect mobility in SG-TFTs.[5,6] To show this effect, we have simulated five n-channel devices with the same geometry and with a single twin boundary in the channel, which is perpendicular to the silicon/gate oxide interface. The devices differ in the angle between the orientation of the twin boundary and the channel direction, which is chosen at five values: 0° (orthogonal to channel direction), 30°, 45°, 60°, and 90° (parallel to channel).

The channel surface potential for the devices with a twin boundary has been observed at different V_{GS} and V_{DS}. There is a potential barrier associated with the twin boundary with a height of ~0.17 eV for $V_{GS}=10$ V and $V_{DS}=0.1$ V, which is much bigger than kT at room temperature $T=300$ K, where k is the Boltzmann constant. So the current across the barrier is limited by thermionic emission. As shown in Fig. 2 and Table I, we find that the effective electron mobility increases for increasing angle between the orientation of the twin boundary and the channel direction, which is consistent with the experiment results reported by Ishihara *et al.*[5,6] A similar effect has been reported for poly-Si TFTs with large grains by Jung *et al.*[8] They found that changing the orientations of grain boundaries can induce a variation of field-effect mobilities of more than a factor of 2, which is comparable with our simulation results.

Another important TFT parameter we want to simulate is the off current. We have found that some SG-TFTs show asymmetrical off current when source and drain are exchanged. As shown in Fig. 3(a), on current shows little change when swapping source and drain, whereas the off current shows a change of one order of magnitude. This phenomenon is not present in small-grain poly-Si TFTs.

We assume that this effect is presumably due to twin boundaries in the channel. A 3D device with a twin boundary in contact with the drain or the source was designed for

TABLE I. Simulated field-effect effective mobilities of 3D single grain TFTs with a single twin boundary in the middle of the channel oriented to a different angle relative to the channel direction.

Angle (deg)	Field-effect mobility (cm^2/V s)
90	684
60	611
45	505
30	492
0	425

Downloaded 19 Aug 2011 to 158.132.161.52. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

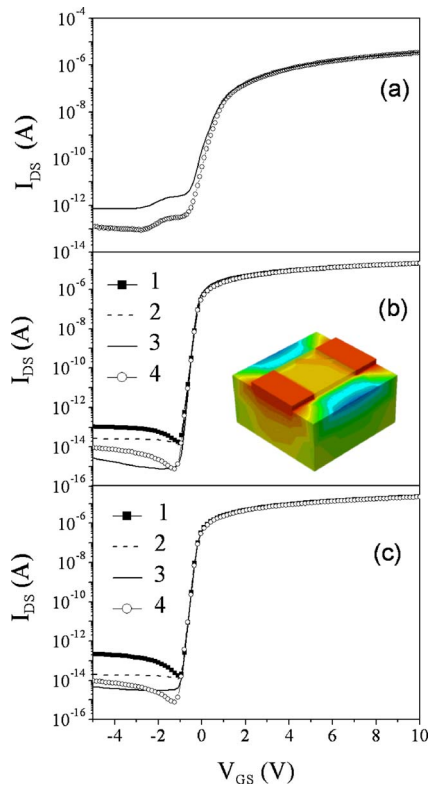

FIG. 3. (a) Transfer characteristics of a SG-TFT (W/L=3.2 μm/2.9 μm) for source and drain exchange. V_{DS}=0.1 V. (b) Simulation of the transfer characteristics of SG-TFT devices with a twin boundary in contact with the drain (curves 1–3)or the source (curve 4). V_{DS}=0.1 V. Curves 1–3 correspond to different densities of trap states in the twin boundary, as shown in Table II. Inset: A SG-TFT without the metal gate and the gate oxide, in which a twin boundary in the channel is in contact with the drain. (c) Simulation of the transfer characteristics of SG-TFT devices with a twin boundary in contact with the drain (curves 1–3)or the source (curve 4). V_{DS}=0.1 V. Curves 1–3 correspond to different capture cross sections of trap states in the twin boundary, as shown in Table III.

simulation, as shown in the inset of Fig. 3(b). The geometric size of this device is identical to the device of Fig. 1. The planar density of trap states and their capture cross in the twin boundary are assumed to be the value given by Eqs. (6) and (7). Then the transfer characteristics of the device are simulated before and after the source/drain swapping. As shown in Fig. 3(b), the off current is much higher if the twin boundary is in contact with the drain. This effect can be easily understood considering that the the off current is controlled by carrier generation near the drain.[12] It is worth pointing out that even if only the edge of a planar trap distribution is in contact with the drain, this yields a remarkable increase of the off current, an effect that can only be accurately simulated in 3D.

TABLE II. Different densities of trap states assumed in the twin boundary in the simulation of single grain TFTs.

Curves	N_{at} ($cm^{-2}\,eV^{-1}$)	N_{ad} ($cm^{-2}\,eV^{-1}$)	N_{dt} ($cm^{-2}\,eV^{-1}$)	N_{dd} ($cm^{-2}\,eV^{-1}$)
1	5×10^{15}	2×10^{11}	5×10^{15}	4.5×10^{11}
2	5×10^{15}	2×10^{12}	5×10^{15}	4.5×10^{12}
3	5×10^{15}	2×10^{13}	5×10^{15}	4.5×10^{13}

TABLE III. Different capture cross sections of trap states assumed in the twin boundary in the simulation of single grain TFTs.

Curves	σ_{na} (cm^2)	σ_{nd} (cm^2)	σ_{pa} (cm^2)	σ_{pd} (cm^2)
1	10^{-13}	10^{-11}	10^{-11}	10^{-13}
2	10^{-15}	10^{-13}	10^{-13}	10^{-15}
3	10^{-16}	10^{-14}	10^{-14}	10^{-16}

In the simulation, we have changed the density of trap states in the grain boundary. Since the main contribution of the electron-hole generation comes from the midgap states, as shown in Table II, N_{at} and N_{dt} are kept constant, while N_{ad} and N_{dd} are changed for two orders of magnitude. So the relative change of midgap states is big, while tail states (the trap states near the conduction band and valence band) have little change. As shown in Fig. 3(b), the off current changes for two orders of magnitude when the twin boundary is in contact with the drain, while there is no obvious change in the transfer characteristics when the twin boundary is in contact with the source. We can find that there is little enhancement in off current by the twin boundary in contact with the drain when the density of trap states in the twin boundary is small (curve 3).

The effect of capture cross section on the off current has also been simulated in the same device. The density of trap states in the twin boundary is given by Eqs. (6) and (7). However, the capture cross sections were changed for three orders of magnitude, as shown in Table III. The corresponding off current, as shown in Fig. 3(c), changes for two orders of magnitude when the twin boundary is in contact with the drain, while there is no change when the boundary is near the source. Therefore, density of states in the midgap and the capture cross section of these traps are important for the off current, which is consistent with the theory for off current reported before.[12] In conclusion, the 3D simulation indicates that an asymmetry in the off current for source-drain swapping will result if a twin boundary is in contact with the drain but not with the source.

[1] T. Sameshima, S. Usui, and M. Sekiya, IEEE Electron Device Lett. **7**, 276 (1986).
[2] R. Ishihara, P. C. Wilt, B. D. Dijk, A. Burtsev, F. C. Voogt, G. J. Bertens, J. W. Metselaar, and C. I. M. Beenakker, Proc. SPIE **4295**, 14 (2001).
[3] P. Ch. Van der Wilt, B. D. van Dijk, G. J. Bertens, R. Ishihara, and C. I. M. Beenakker, Appl. Phys. Lett. **72**, 1819 (2001).
[4] R. Ishihara, Y. Hiroshima, D. Abe, B. D. van Dijk, P. Ch. van der Wilt, S. Higashi, S. Inoue, T. Shimoda, J. W. Metselaar, and C. I. M. Beenakker, *Proceedings of Eurodisplay, 2002*, Vol. 407–409, p. 1.
[5] R. Ishihara, P. Ch. van der Wilt, B. D. van Dijk, J. W. Metselaar, and C. I. M. Beenakker, Proc. SPIE **5004**, 10 (2003).
[6] R. Ishihara, M. He, V. Rana, Y. Hiroshima, S. Inoue, T. Shimoda, J. W. Metselaar, and C. I. M. Beenakker, Thin Solid Films **487**, 97 (2005).
[7] T. Mizuki, J. S. Matsuda, Y. Nakamura, J. Takagi, and T. Yoshida, IEEE Trans. Electron Devices **51**, 204 (2004).
[8] Y. H. Jung, J. M. Yoon, M. S. Yang, W. K. Park, and H. S. Soh, Mater. Res. Soc. Symp. Proc. **621**, Q9.14.1 (2000).
[9] M. Kimura, S. Inoue, T. Shimoda, and T. Eguchi, J. Appl. Phys. **89**, 596 (2001).
[10] A. Benvenuti, M. R. Pinto, J. W. M. Coughran, N. L. Schryer, C. U. Naldi, and G. Ghione, Tech. Dig. - Int. Electron Devices Meet. **1991**, 499.
[11] P. Migliorato, C. Reita, G. Tallarida, M. Quinn, and G. Fortunato, Solid-State Electron. **38**, 2075 (1995).
[12] O. K. B. Lui and P. Migliorato, Solid-State Electron. **41**, 575 (1997).

Downloaded 19 Aug 2011 to 158.132.161.52. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions