Synthesis and memory effect study of Ge nanocrystals embedded in LaAlO$_3$ high-k dielectrics

X. B. Lu, P. F. Lee, and J. Y. Dai[a)]
Department of Applied Physics and Materials Research Center, The Hong Kong Polytechnic University, Hung Hom, Kowloon, Hong Kong, People's Republic of China

A floating gate memory structure utilizing Ge nanocrystals embedded in LaAlO$_3$ (LAO) high-k dielectric films has been fabricated by pulsed-laser deposition. A cross-sectional high-resolution transmission electron microscopy study revealed that the floating gate structure contains 5-nm-diam spherelike Ge nanocrystals embedded in amorphous LAO. A significant memory effect with a very high density of charge storage up to $2 \times 10^{13}/cm^2$ in the Ge nanocrystals and a maximum flat band voltage shift of 3.2 V have been achieved for the trilayer structure of LAO(8 nm)/Ge/LAO(3 nm)/Si. The memory structure utilizing the Ge nanocrystals grown in 1 min showed excellent charge retention characteristics, whereas the decay in memory capacitance after 10^4 s of stress under a flat band voltage was only 8%. These results suggest that this memory structure utilizing Ge nanocrystals embedded in a LAO dielectric offers a high potential for the further scaling of floating gate memory devices. In addition, the effects of Ge growth time, and thus the size and density of the Ge nanocrystals, to the charge storage and charge retention characteristics were also studied. © *2005 American Institute of Physics.* [DOI: 10.1063/1.1926414]

Metal–oxide–semiconductor (MOS) memory structures based on Si quantum dots or nanocrystals have recently attracted a great deal of interest due to the physical phenomena and potential applications in scaled flash memory.[1–4] In this kind of memory structure, Si nanocrystals are embedded as charge-storage nodes in an oxide layer between the control gate and the tunneling layer, which can reduce the problem of charge loss encountered in conventional flash memories. It allows thinner injection oxides and, hence, smaller operating voltages, better endurance, and faster write/erase speeds.[1,2] The memory function of these devices has been attributed to the charge exchange between the nanocrystals and inversion layer. Most quantum dot flash memories use Si nanocrystals to replace the continuous floating gate layer. However, research results in several groups have demonstrated the superior properties of Ge-based nanocrystal memories over those based on Si.[4–6] The Ge nanocrystals offer improved nonvolatile charge retention time due to their smaller band gap. The smaller band gap provides both a higher confinement barrier for the retention mode and a smaller barrier for the program and erase modes. Various methods of fabrication have been reported to form the Ge dot, such as implantation of Ge ions in SiO$_2$,[7] the sputter deposition of Ge on the Si substrate,[8] and the rapid thermal annealing of chemical–vapor–deposited Ge layers.[9] Pulsed–laser deposition (PLD) has also proven to be very successful in the fabrication of complex oxide materials, and is also effective in the growth of Ge nanocrystals.

High-k gate dielectrics have been extensively investigated for replacing SiO$_2$ in future MOS field effect transistors (MOSFETs).[10–12] In recent studies, high-k gate dielectrics were also used as the control and tunneling oxide layers in floating gate memory structures,[9,13–15] which allow for a thinner equivalent oxide thickness (EOT) without sacrificing nonvolatility. Furthermore, the thicker physical thickness of the high-k dielectrics ensures good retention characteristics, while due to the unique band alignment of the high-k dielectric with Si, a lower electron barrier height allows high currents across the tunneling oxide to be obtained at a low control gate voltage during the programming. As one of the potential high-k gate dielectrics to replace SiO$_2$, LaAlO$_3$ (LAO) has been extensively studied because of its many advantages such as a medium dielectric constant, a high band offset with Si, and good thermal stability when in contact with Si.[16–18] Furthermore, it exhibits good process compatibility with the current standard complementary metal–oxide semiconductor (CMOS) technology.[19] In this Letter, LAO is used as the control and tunneling oxide layers in the trilayer memory structure of LAO/Ge/LAO/Si fabricated by PLD.

After wet-chemical cleaning, the p-type (100) Si substrate with $\rho = 4 \sim 6$ Ω cm was dipped into an HF (10%) solution for 60 s to remove the amorphous SiO$_2$ layer from the silicon surface, leaving a hydrogen-terminated surface. The Si substrate was then immediately moved into the PLD chamber with a maximum base pressure of 2×10^{-5} Pa. Before the film deposition, the substrate was heated to 400 °C. Then, oxygen ambient was introduced until the pressure in the chamber reached 0.2 Pa and the deposition was started. First, a very thin LAO layer was deposited at 400 °C as the tunneling oxide. After the deposition of the tunneling oxide, Ge nanocrystals were deposited in a 1×10^{-4} Pa vacuum. Finally, the trilayer memory structure was built by the deposition of another thicker layer of LAO onto the Ge nanocrystals as the control oxide layer. The sample was *in situ* annealed in pure N$_2$ ambient at an elevated temperature of 750 °C for 30 min. Pt top electrodes with an area of 3.14 $\times 10^{-4}$ cm^2 were deposited on the surface of the samples using a shadow mask to fabricate the MOS memory structures. The hysteresis loop and the charge retention characteristics of the MOS capacitors were evaluated by capacitance–voltage (C–V) measurements with an Agilent 4294A impedance analyzer at room temperature. The cross-sectional
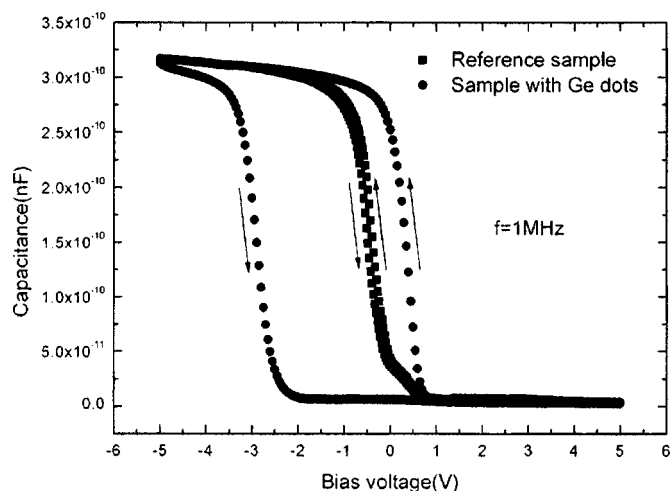
---

a)Electronic mail: apdaijy@inet.polyu.edu.hk

FIG. 1. C–V hysteresis curves of memory capacitors with 1 min Ge nanocrystal deposition and reference sample without Ge nanocrystals.

FIG. 3. C–V hysteresis curves of memory capacitors with different deposition time of Ge nanocrystals.

structures of the trilayer memory stack were characterized by high-resolution transmission electron microscopy (HRTEM).

Figure 1 shows the typical high-frequency C–V curves of two MOS capacitors with and without Ge nanocrystals. In the sample with Ge nanocrystals, the thicknesses of the control and tunneling oxide layers are about 3 and 8 nm, respectively, and the time of Ge nanocrystals deposition is 1 min. It can be seen that the sample with Ge nanocrystals exhibits an anticlockwise C–V hysteresis loop and a very large flat band voltage shift of 3.2 V. By contrast, the control sample without Ge nanocrystals shows no obvious flat band voltage shift, suggesting that the large memory effect observed in the sample containing Ge nanocrystals is produced by the charges stored in the Ge nanocrystals. Generally, the hysteresis may be introduced by the mixed effects of injected charges stored in the nanocrystals, essential trap charges existing in the oxide or interface states.[15] Since the processes for fabricating the two samples are the same except for the Ge nanocrystals, the hysteresis effect produced by the essential trap charges and interfacial states should be the same for the two samples, and can, therefore, be ruled out. It is also worth noting that the equivalent oxide thickness (EOT) to SiO_2 of the memory structure is calculated to be 3.3 nm, for a total oxide thickness of 11 nm of the structure. This will be beneficial for the integration of this large memory structure into smaller scale devices.

Figures 2(a) and 2(b) show the cross-sectional HRTEM images of the trilayer memory structures with 1- and 2-min Ge deposition, respectively. The Ge nanocrystals embedded
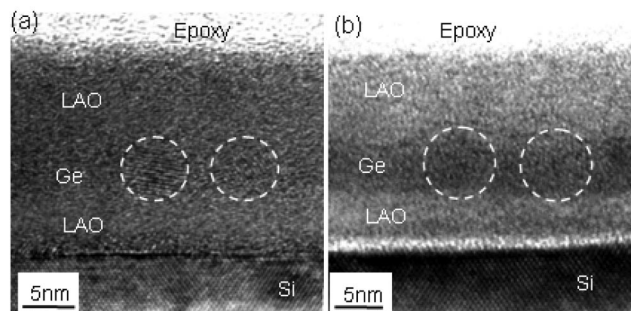

FIG. 2. Cross-sectional HRTEM images of the trilayer memory structure. (a) 1-min Ge deposition; (b) 2-min Ge deposition.
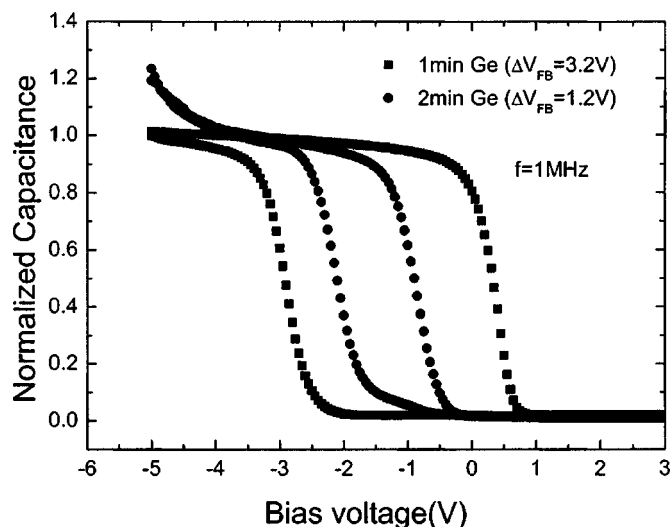
in LAO can be clearly seen between tunnel oxide and control oxide, and the shape of the Ge nanocrystals is almost spherical. The diameters of the Ge nanocrystals are approximately 5 and 7.5 nm, respectively, for 1- and 2-min deposition of Ge. Based on the C–V results shown in Fig. 1, the maximum stored charge density can be up to $2.06 \times 10^{13}/cm^2$, as estimated by the formula given by Tiwari[1] and Kim et al.,[5] which is large enough to meet the requirements of the future flash memory application.

In order to investigate the relation between the storage charge density, and thus the flat band voltage shift, with the nanocrystal density embedded in the oxide layer, we also deposited Ge nanocrystals for a longer time of 2 min, expecting a larger density of Ge nanocrystals. The C–V hysteresis curves of the samples with 1- and 2-min Ge depositions are shown in Fig. 3, where large hysteresis loops can be observed for both samples, indicating a strong charge storage effect in them. But contrary to expectations, the flat band voltage shift for the sample with a longer Ge deposition time of 2 min is only 1.2 V, which is much smaller than that of the sample with a 1-min Ge deposition (3.2 V). We speculate that this decrease in the flat band voltage shift for the longer Ge deposition sample is due to the decrease in the nanocrystal density in the sample. As can be seen from Fig. 2(b), the Ge nanocrystals deposited for 2 min resulted in a more continuous Ge layer with a larger grain size and a shorter space between the grains, and thus a smaller density of Ge nanocrystals. Therefore, if one Ge nanocrystal stores only one electron, the storage charges decrease with the decrease in the density of the Ge nanocrystal. So the flat band voltage shift decreases for the sample with the 2-min Ge deposition.

The memory data retention characteristics at room temperature for the trilayer memory capacitors were also studied. The memory capacitors were first charged for 15 s at a bias voltage of 10 V. Then, the capacitance decay measurement was carried out under a −1 V bias voltage. Figure 4 shows the normalized capacitance–time (C–t) curves of the samples with a 1- and 2-min Ge deposition. It can be seen that after 10^4 seconds of stress, the decayed capacitance for the memory capacitor with a 1-min Ge deposition is only 8%, suggesting very good charge retention characteristics. However, for the sample with a 2-min Ge deposition, rapid
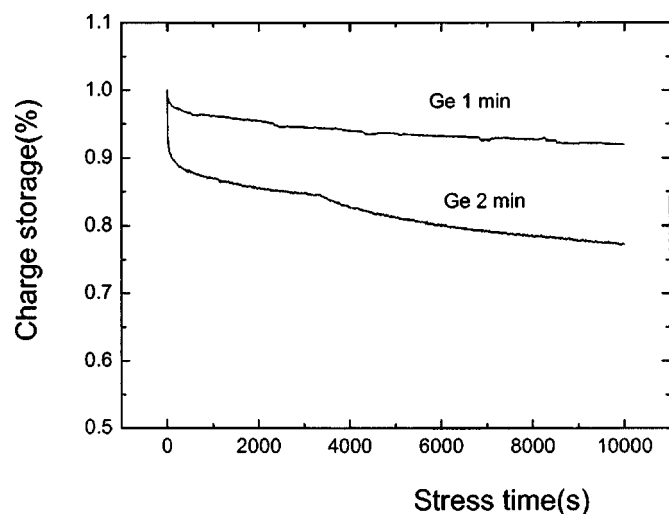
FIG. 4. Normalized capacitance decay characteristics for samples with a 1- and 2-min Ge nanocrystals deposition.

decay can be clearly observed at the beginning of the stress. The drop in capacitance after 10^4 seconds of stress is about 23%.

For the fast decay in the capacitance of the floating gate memory structure, some possible mechanisms have been proposed earlier. One is the lateral channel leakage mechanism, proposed by Kim;[5] and another is the Coulomb repulsion of several electrons in nanocrystals, proposed by Winkler et al.[20] According to the HRTEM results in Fig. 2 and the discussion of the results illustrated in Fig. 3, the Ge layer in the sample with a 2-min Ge deposition is more continuous than that of the sample with an 1 min Ge deposition. If the fast decay in our samples is due to the lateral charge leakage, the sample with a more continuous Ge layer should have a larger lateral charge leakage and thus worse charge retention characteristics. As can be seen from Fig. 4, the sample with a 1-min Ge deposition has better charge retention characteristics than the sample with a 2-min Ge deposition. This experimental result is consistent with the mechanism of lateral charge leakage, suggesting that the lateral channels exist inside the Ge layer, leading to charge leakage and thus to the fast decay of the capacitance of the memory capacitor. The later slow decay may be due to the electron tunneling back to the channel via the tunneling barrier.

In summary, the trilayer memory structure of Ge nanocrystals embedded in a LAO high-k dielectric was fabricated and characterized. High-density Ge nanocrystals with a di-ameter of around 5 nm were fabricated by pulsed laser deposition. Good performances in terms of charge storage and data retention were observed for this trilayer memory structure. The memory capacitor with a 1-min Ge deposition has better charge retention characteristics and a larger hysteresis loop width than the memory capacitor with a 2-min Ge deposition. The fast capacitance decay in the memory structure may be mainly due to the lateral charge loss.

[1]S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan, Appl. Phys. Lett. **68**, 1377 (1996).
[2]S. Tiwari, F. Rana, K. Chan, L. Shi, and H. Hanafi, Appl. Phys. Lett. **69**, 1232 (1996).
[3]Y. Shi, K. Saito, H. Ishikuro, and T. Hiramoto, J. Appl. Phys. **84**, 2358 (1998).
[4]Y. C. King, T. J. King, and C. Hu, IEEE Trans. Electron Devices **48**, 696 (2001).
[5]J. K. Kim, H. J. Cheong, Y. Kim, J. Y. Yi, and H. J. Bark, Appl. Phys. Lett. **82**, 2527 (2003).
[6]M. Kanoun, A. Souifi, T. Baron, and F. Mazen, Appl. Phys. Lett. **84**, 5079 (2004).
[7]K. S. Min, K. V. Shcheglov, C. M. Yang, H. A. Atwater, M. L. Brongersma, and A. Polman, Appl. Phys. Lett. **68**, 2511 (1996).
[8]M. Zacharias, R. Weigand, B. Dietrich, F. Stolze, J. Bläsing, P. Veit, T. Drüsedau, and J. Christen, J. Appl. Phys. **81**, 2384 (1997).
[9]D. W. Kim, T. Kim, and S. K. Banerjee, IEEE Trans. Electron Devices **50**, 1823 (2003).
[10]G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **89**, 5243 (2001).
[11]A. I. Kingon, J.-P. Maria, and S. K. Streiffer, Nature (London) **406**, 1032 (2000).
[12]H.-J. Cho, C. S. Kang, K. Onishi, S. Gopalan, R. Nieh, R. Choi, S. Krishnan, and J. C. Lee, IEEE Electron Device Lett. **23**, 249 (2002).
[13]R. Gupta, W. J. Yoo, Y. Q. Wang, Z. Tan, G. Samudra, S. J. Lee, D. S. H. Chan, K. P. Loh, L. K. Bera, N. Balasubramanian, and D. L. Kwong, Appl. Phys. Lett. **84**, 4331 (2004).
[14]J. J. Lee, X. G. Wang, W. P. Bai, N. Lu, and D.-L. Kwong, IEEE Trans. Electron Devices **50**, 2067 (2003).
[15]Q. Wan, N. L. Zhang, W. L. Liu, C. L. Lin, and T. H. Wang, Appl. Phys. Lett. **83**, 138 (2003).
[16]X. B. Lu, X. Zhang, R. Huang, H. B. Lu, Z. H. Chen, W. F. Xiang, M. He, B. L. Cheng, H. W. Zhou, X. P. Wang, C. Z. Wang, and B. Y. Nguyen, Appl. Phys. Lett. **84**, 2620 (2004).
[17]L. F. Edge, D. G. Schlom, S. A. Chambers, E. Cicerrella, J. L. Freeouf, B. HollÄnder, and J. Schubert, Appl. Phys. Lett. **84**, 726 (2004).
[18]B.-E. Park and H. Ishiwara, Appl. Phys. Lett. **82**, 1197 (2003).
[19]X. B. Lu, H. B. Lu, Z. H. Chen, X. Zhang, R. Huang, H. W. Zhou, X. P. Wang, C. Z. Wang, B. Y. Nguyen, W. F. Xiang, M. He, and B. L. Cheng, Appl. Phys. Lett. **85**, 3543 (2004).
[20]O. Winkler, F. Merget, M. Heuser, B. Hadam, M. Baus, B. Spangenberg, and H. Kurz, Microelectron. Eng. **61**, 497 (2002).