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Interfacial and electrical properties of InGaAs metal-oxide-semiconductor capacitor with TiON/TaON multilayer composite gate dielectric

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InGaAs metal-oxide-semiconductor (MOS) capacitors with composite gate dielectric consisting of Ti-based oxynitride (TiON)/Ta-based oxynitride (TaON) multilayer are fabricated by RF sputtering. The interfacial and electrical properties of the TiON/TaON/InGaAs and TaON/TiON/InGaAs MOS structures are investigated and compared. Experimental results show that the former exhibits lower interface-state density ($1.0 \times 10^{12}\,cm^{-2}\,eV^{-1}$ at midgap), smaller gate leakage current (9.5×10^{-5} A/cm^2 at a gate voltage of 2 V), larger equivalent dielectric constant (19.8), and higher reliability under electrical stress than the latter. The involved mechanism lies in the fact that the ultrathin TaON interlayer deposited on the sulfur-passivated InGaAs surface can effectively reduce the defective states and thus unpin the Femi level at the TaON/InGaAs interface, improving the electrical properties of the device. © *2015 AIP Publishing LLC*.
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In recent years, InGaAs has been extensively investigated as an alternative channel material of n-type metal-oxide-semiconductor field-effect transistors (n-MOSFETs) for next-generation nanoscale complementary MOS device applications with low power and high speed due to its higher electron mobility than that of Si.[1] Meanwhile, many high-k gate dielectric materials (e.g., HfO_2,[2] TiO_2,[3] and La_2O_3[4]) have been widely investigated as the gate dielectric of InGaAs MOS devices. However, direct deposition of high-k dielectric on InGaAs yields poor electrical characteristics due to easy formation of native oxide on the InGaAs surface, resulting in an extremely high density of interface states and thus inducing Fermi-level pinning at the high-k/InGaAs interface. So, the use of an interfacial passivation layer (IPL) (e.g., Si,[2] Ge,[5] SiO_xN_y,[6] and Al_2O_3[7]) prior to high-k deposition on InGaAs has been extensively studied, achieving improved interface quality and electrical properties for the device. However, the performance improvement comes at the cost of extra processing time, scaling limitation, and complex IPL. To obtain a high-quality interface without an IPL, Suri *et al*. investigated an engineered HfAlO gate dielectric formed on sulfur-passivated GaAs by alternating layers of atomic-layer deposited Al_2O_3 and HfO_2, obtaining excellent interface with GaAs and improved device characteristics.[8] However, the k value of Al_2O_3 is low (~9),[9] which limits further device scaling. Ta-based oxynitride (TaON) with a higher k value (~26) than HfO_2 has been used in GaAs MOSFETs and showed excellent electrical and reliability properties.[10] Ti-based oxynitride (TiON) has an even higher k value (~80) but larger leakage current.[9] Moreover, it has been demonstrated that the TaO-TiO multilayer structure as gate dielectric on Si and Ge substrates has excellent electrical properties.[11,12] Therefore, in this work, multiple layers of alternate TaON and TiON are deposited on InGaAs by alternately sputtering Ti and Ta targets, and the interfacial and electrical properties of MOS capacitors with the TiON/TaON or TaON/TiON multilayer as gate dielectric are investigated. As a result, excellent electrical properties are achieved with small gate leakage current, low interface-state density, and high device reliability for the InGaAs MOS device with TiON/TaON multilayer.

InGaAs MOS capacitors were fabricated on an *n*-type $In_{0.53}Ga_{0.47}As$ epilayer with a Si doping of $2\sim3 \times 10^{16}\,cm^{-3}$ grown on an n^+-InP (100) substrate. The wafers were degreased using acetone, ethanol, and isopropanol and cleaned in diluted HF solution (5%) for 2 min to remove the native oxide, followed by dipping in $(NH_4)_2S$ solution (8%) for 20 min at room temperature for sulfur passivation of the InGaAs surface and then rinsing in de-ionized water for 5 cycles. After N_2 drying, the wafers were immediately transferred to a sputtering chamber. A high-k composite gate dielectric (~5 nm) of 10 TiN/TaN or TaN/TiN layers (~0.5 nm per layer) was deposited by alternately RF-sputtering Ti and Ta targets in an Ar/N_2 (24 sccm/12 sccm) ambient at room temperature. A post-deposition annealing (PDA) was performed at 600 °C for 60 s in N_2 (500 sccm) + O_2 (50 sccm) to convert the TaN and TiN layers to TaON and TiON, respectively, to form two kinds of MOS devices (denoted as TiON/TaON/InGaAs and TaON/TiON/InGaAs samples, respectively). Finally, Al was thermally evaporated and patterned as the gate electrode and also as back electrode of the devices, followed by forming-gas (5% H_2 + 95% N_2) annealing at 300 °C for 20 min to reduce their contact resistance.

High-frequency (HF, 1-MHz) capacitance-voltage (C-V) and gate leakage current density vs. gate voltage

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(J_g-V_g) curves of the samples were measured using HP4284A precision LCR meter and HP4156A semiconductor parameter analyzer, respectively. Physical thickness of the gate dielectric was measured by ellipsometry. X-ray photoelectron spectroscopy (XPS) was used to examine the chemical states at/near the high-k/InGaAs interface.

Fig. 1 shows the HF (1-MHz) C-V curves of the two samples. It can be obviously seen that the accumulation capacitance drops for the TaON/TiON/InGaAs sample under large positive gate voltage due to large leakage current, which probably comes from a high density of defective states at the conduction-band edge of InGaAs caused by a considerable amount of In-/Ga-/As-O and As-As bonds at the TiON/InGaAs interface.[10,13] However, for the TiON/TaON/InGaAs sample, the accumulation capacitance exhibits a quasi-saturation as the positive gate voltage increases, which should be ascribed to the improved interfacial properties associated with the suppressed growth of a unstable low-k interfacial layer (In/Ga/As oxides) at the InGaAs surface achieved by the ultrathin TaON IPL on the InGaAs surface, as confirmed by the XPS analysis below. The interface-state density (D_{it}) at midgap extracted from the 1-MHz C-V curve is $1.0 \times 10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ for the TiON/TaON/InGaAs sample by using the Terman's method and is much lower than that for the TaON/TiON/InGaAs sample ($7.1 \times 10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$). A smaller negative shift of the flatband voltage (V_{fb}) for the TiON/TaON/InGaAs sample (−0.32 V) than the TaON/TiON/InGaAs sample (−0.44 V) in Fig. 1 implies a greatly reduced positive equivalent oxide-charge density (Q_{ox}) ($4.9 \times 10^{11}\,\mathrm{cm}^{-2}$ *vs.* $4.0 \times 10^{12}\,\mathrm{cm}^{-2}$) associated with interface and near-interface traps. This is attributed to less out-diffusions of In, Ga, and As atoms from the substrate to the high-k layer due to the blocking role of the ultrathin TaON IPL in the TiON/TaON/InGaAs sample.[14] The equivalent k value of the gate dielectric can be calculated as $C_{ox}T_{ox}/\varepsilon_0$, where C_{ox} is accumulation capacitance per unit area and T_{ox} is the total physical thickness of the gate dielectric. T_{ox} of the TiON/TaON/InGaAs and TaON/TiON/InGaAs samples measured by ellipsometry is 3.9 nm and 3.6 nm, respectively. So, a slightly larger equivalent k value of 19.8 is achieved for the former than the latter (19.6) due to suppressed oxygen diffusion from the high-k gate dielectric to the InGaAs surface by the TaON interlayer and thus less formation of the low-k interfacial oxide.

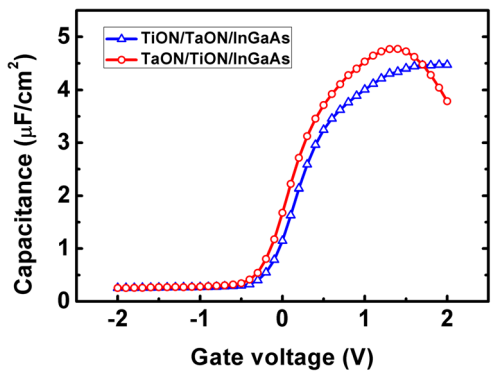

FIG. 1. HF (1-MHz) C-V curve for the TiON/TaON/InGaAs and TaON/TiON/InGaAs samples.

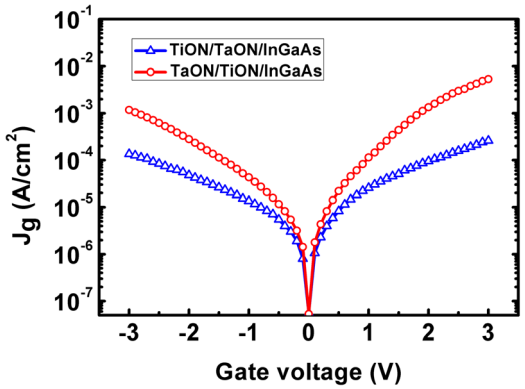

FIG. 2. Gate leakage current density (J_g) *vs.* gate voltage (V_g) for the two samples.

The gate leakage properties of the two samples are shown in Fig. 2. Large gate leakage current density is observed for the TaON/TiON/InGaAs sample, e.g., 1.3×10^{-3} A/cm^2 at $V_g = 2$ V. However, for the TiON/TaON/InGaAs sample, the leakage current density is greatly reduced, e.g., 9.5×10^{-5} A/cm^2 at $V_g = 2$ V. The smaller gate leakage current of the latter is closely related to its smaller Q_{ox} and D_{it}. In addition, a high-field stress at 3 MV/cm [$=(V_g - V_{fb})/T_{ox}$] for 3000 s is used to examine the reliability of the samples. The J_g-V_g properties are measured before and after the stressing, as shown in Fig. 3. As shown in Fig. 4, the increased gate leakage current after the stress for the two samples could come from carrier charging at the pre-existing traps of the oxide layer and also from the trap-assisted tunneling of electrons via interface and near-interface traps generated by the stress.[15,16] Obviously, the post-stress increase of the leakage current is smaller for the TiON/TaON/InGaAs sample than the TaON/TiON/InGaAs sample, which can be associated with less stress-induced generation of interface and near-interface traps due to less weak In/Ga/As-O bonds at/near the TaON/InGaAs interface mentioned earlier. In addition, it is worth pointing out that under the high-field stress, the electric field would induce an additional tensile stress to the InGaAs epilayer due to the inverse piezoelectric effect of InGaAs,[17–19] and the strained layer would relax through crystallographic defect formation. The created defects could be electrically active and provide a path for gate leakage current, resulting in device degradation.[19]

In order to further identify the effects of the IPL on the chemical states at the interface between the high-k dielectric

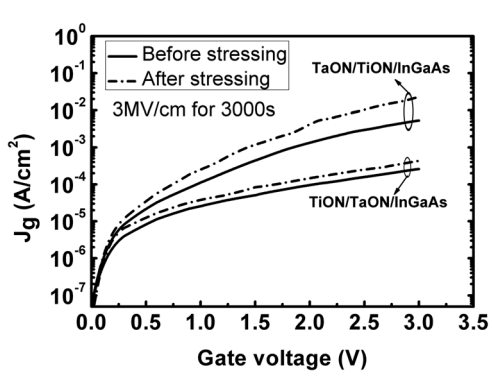

FIG. 3. Gate leakage current density (J_g) of the two samples before and after a high-field stress at 3 MV/cm for 3000 s.

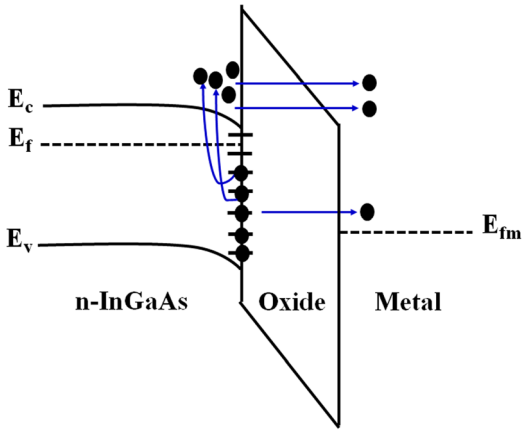

FIG. 4. The schematic diagram of interface-trap-assisted tunneling under positive gate voltage.

and InGaAs substrate, the In 3d, Ga 3d, and As 2p spectra of the two samples are analyzed by XPS, as shown in Figs. 5, 6, and 7. The In-S, Ga-S, and As-S peaks are clearly observed in the In 3d, Ga 3d, and As 2p spectra of the samples. It has been reported that sulfur passivation of the InGaAs surface is beneficial for suppressing the formation of In/Ga/As-O bonds[6,13] but cannot fully eliminate them. In Fig. 5, an In-O peak occurs for the TiON/TaON/InGaAs and TaON/TiON/InGaAs samples, and its content at the interface is calculated to be 1.6% and 5.7%, respectively, based on the In-O/In$3d_{5/2}$ peak-area ratio. Obviously, the content of In-O bond is lower for the former than the latter, implying that the formation of In oxide at the interface can be more effectively suppressed by the ultrathin TaON IPL than the ultrathin TiON IPL. Similarly from Fig. 6, the content of Ga-O bond for the TiON/TaON/InGaAs sample (14.2% from the Ga-O/Ga3d peak-area ratio) is lower than that for the TaON/TiON/InGaAs sample (29.2%). Furthermore, as shown in Fig. 7, As-O bond occurs only in the TaON/TiON/InGaAs sample (its content is 1.9% from the As-O/As2p peak-area ratio) but disappears in the TiON/TaON/InGaAs sample. Such a low content of As-O bond at the TiON/InGaAs interface should be due to the decomposition of As oxide to Ga oxide, In oxide, and elemental As ($2As_2O_3 + 2InGaAs \rightarrow Ga_2O_3 + In_2O_3 + 6As$) during the PDA, which also explains the high content of Ga-O and In-O bonds at the interface.[20] Moreover, the intensity of the As-As peak for the TiON/TaON/InGaAs sample (a content of 3.6% from the As-As/As2p peak-area ratio) is lower than that for the TaON/TiON/InGaAs sample (a content of 5.7%). This indicates that the TaON IPL on the sulfur-passivated InGaAs surface can more effectively suppress the formation of weak In-O, Ga-O, As-As, and especially As-O bonds than the TiON IPL. Therefore, the TiON/TaON multilayer structure as the gate dielectric of InGaAs MOS device can more effectively reduce the defective states in the bandgap of InGaAs caused by In-O, Ga-O, As-O, and As-As bonds and thus suppress the Femi-level pinning at the TaON/InGaAs interface, resulting in smaller flatband-voltage shift, lower gate leakage current, and higher device reliability, as shown in Figs. 1–3, respectively.

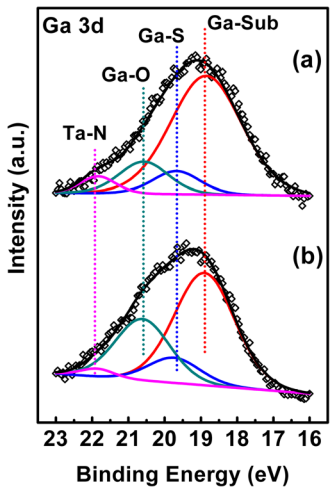

FIG. 6. Ga 3d XPS spectra of the two samples. (a) TiON/TaON/InGaAs and (b) TaON/TiON/InGaAs.

In summary, the interfacial and electrical properties of InGaAs MOS device with composite gate dielectric deposited by sputtering TaON/TiON or TiON/TaON multilayer have been investigated. It is demonstrated that the TiON/TaON-multilayer structure exhibits better performance than

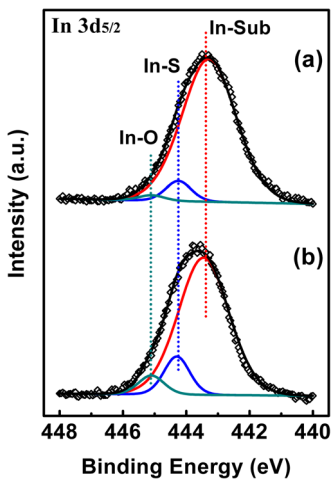

FIG. 5. In 3d5/2 XPS spectra of the two samples. (a) TiON/TaON/InGaAs and (b) TaON/TiON/InGaAs.

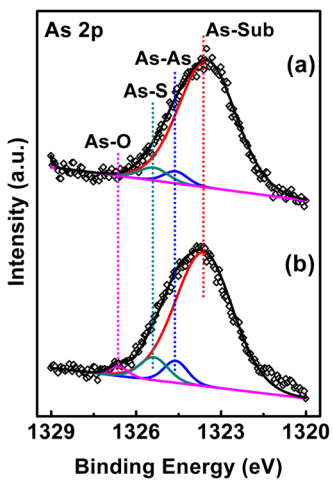

FIG. 7. As 2p XPS spectra of the two samples. (a) TiON/TaON/InGaAs and (b) TaON/TiON/InGaAs.

the TaON/TiON-multilayer structure, e.g., lower interface-state density ($1.0 \times 10^{12}\,cm^{-2}\,eV^{-1}$ at midgap), smaller gate leakage current (9.5×10^{-5} A/cm^2 at $V_g = 2$ V), larger equivalent k value (19.8), and better reliability under electrical stress. All of these could be attributed to the fact that the ultrathin TaON interlayer formed on the InGaAs surface can effectively suppress the formation of interfacial In/Ga/As oxides and also remove excess As atoms, resulting in less interfacial and near-interface traps and thus less Fermi-level pinning at the TaON/InGaAs interface.

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