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Defect states and charge trapping characteristics of HfO_2 films for high performance nonvolatile memory applications

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In this work, we present significant charge trapping memory effects of the metal-hafnium oxide-SiO_2-Si (MHOS) structure. The devices based on 800 °C annealed HfO_2 film exhibit a large memory window of ~5.1 V under ±10 V sweeping voltages and excellent charge retention properties with only small charge loss of ~2.6% after more than 10^4 s retention. The outstanding memory characteristics are attributed to the high density of deep defect states in HfO_2 films. We investigated the defect states in the HfO_2 films by photoluminescence and photoluminescence excitation measurements and found that the defect states distributed in deep energy levels ranging from 1.1 eV to 2.9 eV below the conduction band. Our work provides further insights for the charge trapping mechanisms of the HfO_2 based MHOS devices. © *2014 AIP Publishing LLC*.
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Recently, charge trapping flash (CTF) type memory using a dielectric layer as the charge storage medium has received great attentions as a promising memory technology to replace the traditional floating-gate memories.[1–6] In comparison with the conventional poly-silicon floating gate flash memory, they offer the advantages of smaller cell size, lower program/erase (P/E) voltage, and better reliability.[1–6] The well known CTF type memory is the silicon-oxide-nitride-silicon (SONOS) structure based device.[3,4] Although it has been well developed in recent years, it still suffers from the trade-off between programming speed and data retention:[7,8] on the one hand, thin tunnel oxide layer can enhance the write/erase speed of the SONOS memory device; on the other hand, thicker tunnel oxide can elongate the retention time. To solve these problems in SONOS type CTF memory, CTF memory devices using high-k materials such as HfO_2, Al_2O_3, ZrO_2, etc., have been developed in recent years.[9–15] These devices can provide large band offset with respect to Si, high trap density, and small equivalent oxide thickness (EOT). Therefore, the CTF memory device with high-k film is expected to offer better device performance as compared to the conventional CTF device with Si_3N_4 film.

In this paper, we investigate the memory characteristics of high-k HfO_2 based CTF memory device of Au/HfO_2/SiO_2/Si (MHOS), where the HfO_2 layer works as both charge-trapping oxide and block oxide. Although CTF memory devices without block oxide have been studied by several groups,[7,16] the charge trapping characteristics and mechanisms are still not well understood, and the reported electrical properties remain relatively low. Our present work further clarifies the charge trapping mechanisms of the MHOS memory devices and demonstrates the excellent memory characteristics obtained by a simple fabrication procedure.

P-type Si (100) substrates with $\rho = 1$–$10\,\Omega$ cm were first cleaned by wet-chemical solution and then dipped in a diluted HF solution (1%) to remove the surface oxide; the wafers were then immediately loaded into a vacuum chamber for deposition. The HfO_2 film was deposited by electron-beam evaporation with the substrate temperature of 300 °C. The film thickness was *in-situ* monitored by a crystal thickness monitor and a typical growth rate was around 0.01 nm/s. After deposition, the HfO_2 films were annealed at high temperatures of 800 °C and 875 °C in O_2 atmosphere for 5 min by rapid thermal annealing. For measurements of the electrical properties, dot-shaped Au top electrodes with an area of $\sim 3.14 \times 10^{-4}$ cm^2 were deposited on the surface of the samples using a shadow mask by vacuum evaporation. The electrical properties of the Au-HfO_2-SiO_2-Si capacitors were investigated by an Agilent E4980A impedance analyzer and an Agilent B1500A high-precision semiconductor analyzer at room temperature. High-resolution transmission electron microscopy (HRTEM) was used to study the microstructure of the HfO_2 films. The photoluminescence (PL) and photoluminescence excitation (PLE) measurements were carried out to investigate the features of the defect states in the HfO_2 films.

Figure 1(a) schematically represents the MHOS memory device, where the HfO_2 film was fabricated directly on the HF etched silicon substrate under $\sim 4.0 \times 10^{-4}$ Pa vacuum. The as-deposited HfO_2 film was annealed at high temperature in O_2 ambient by rapid thermal annealing, in order to reduce the leakage current. Figures 1(b) and 1(c) show the cross-sectional TEM images of the HfO_2 films annealed at 800 °C and 875 °C, respectively. Both the high-k HfO_2 films show a fully polycrystalline characteristic and a thickness of ~55 nm. Between the HfO_2 film and the Si substrate, an amorphous SiO_2 layer is clearly observed. The SiO_2 layer's thickness is ~3.0 nm for the sample annealed at 800 °C, while it is ~3.9 nm for the sample annealed at 875 °C. The interfacial

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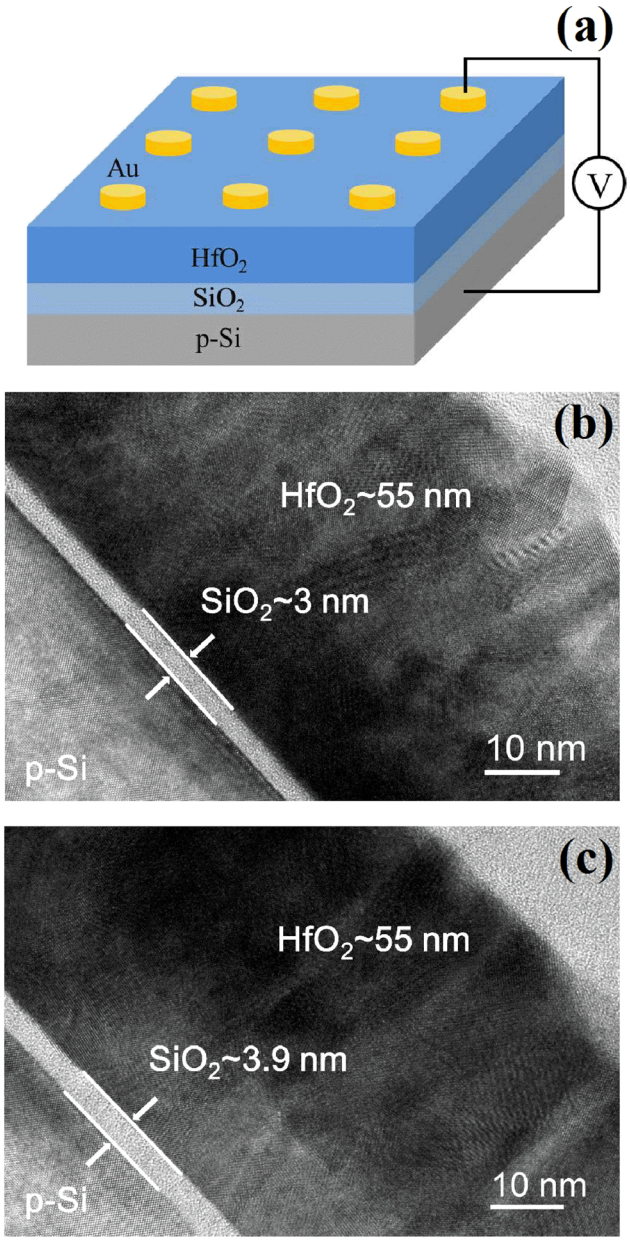

FIG. 1. A schematic diagram of the MHOS device structure (a); cross-sectional HRTEM images for HfO_2 films annealed at 800 °C (b) and 875 °C (c).

SiO_2 layer is undesirable for obtaining small EOT when the high-*k* dielectrics are used as gate dielectric for metal-oxide-silicon field effect transistor[17] or buffer layer for ferroelectric-gate field effect transistor[18] applications. However, this interfacial SiO_2 layer during high-*k* oxide growth or annealing plays a critical role to obtain good electrical properties of the present MHOS devices. The MHOS devices without SiO_2 tunnel oxide layer were also fabricated by using room temperature deposited HfO_2 film without annealing process. Although large memory window was observed, the charge retention time of the MHOS devices was shorter than 10 min (data not shown here). Furthermore, the TEM results also indicate that the SiO_2 tunnel oxide thickness can be controlled by the annealing temperature, which does not require additional processes as used in the previous work.[7] Our present results provide a very simple and low cost method for fabricating the MHOS memory devices.

To study the memory properties of the Au/HfO_2/SiO_2/Si devices, the high frequency (1 MHz) capacitance-voltage (CV) measurements were carried out at room temperature. Figure 2(a) shows the typical CV characteristics of the MHOS devices with HfO_2 film annealed at 800 °C under different sweeping voltages. The anticlockwise direction of the CV hysteresis during positive-negative-positive voltage

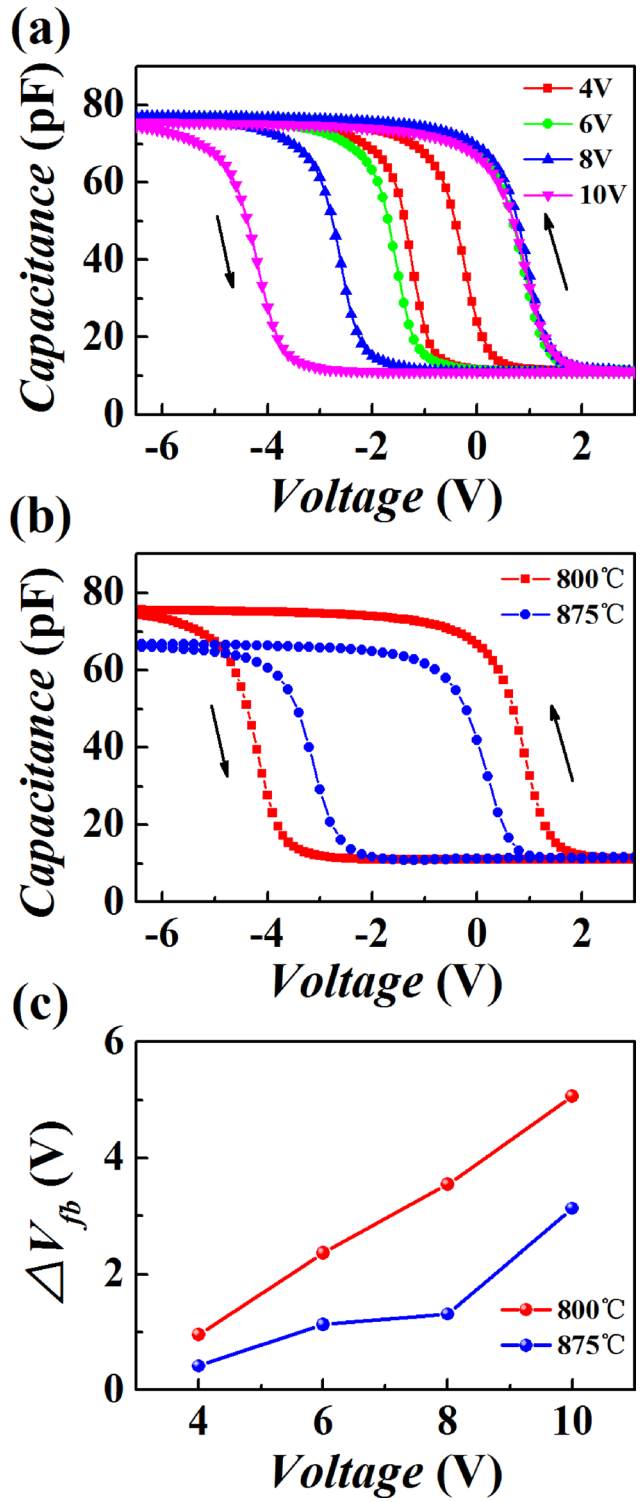

FIG. 2. (a) High frequency (1 MHz) C-V characteristics of the MHOS device with HfO_2 film annealed at 800 °C under different sweeping voltages; (b) typical C-V characteristics of MHOS devices for HfO_2 annealed at 800 °C and 875 °C; (c) impact of annealing temperature on the memory window width of the MHOS devices under different sweeping voltages.

scanning cycle demonstrates the typical hysteresis loop directions of charge trapping. The memory window increases with increasing the sweeping voltages, and a large memory window of 5.1 V under ±10 V sweeping voltage was observed, indicating the significant charge trapping effects in the HfO_2 trapping layer. When further increasing the sweeping voltages above 10 V, the memory window started to show saturation tendency, and it reached the maximum value under 16 V. Under 18 V sweeping voltages, the memory window decreased significantly due to large leakage current. A noticeable feature shown in Fig. 2(a) is that V_{fb} at the positive side saturates even further increasing the positive sweeping voltages. Similar to the charge trapping devices reported by Lee *et al.*,[19] there may also be electron transport from the defect states to the top electrodes during positive voltage sweeping cycles. When the number of the electrons newly trapped in the defect states under the positive voltage is equal to the number of the electrons escaped from the defects, V_{fb} will be saturated even with further increasing the sweeping voltages. The asymmetric hysteresis shown in Fig. 2(a) can be attributed to the different work functions of Au and Si, as well as to the V_{fb} saturation in the positive voltage side. When the annealing temperature increased to 875 °C, the memory window decreased to 3.4 V (shown in Fig. 2(b)), implying that the charge trapping effect is closely related to the annealing temperature. Figure 2(c) shows a comparison of the MHOS devices with 800 °C and 875 °C annealed HfO_2 films under different sweeping voltages. For both samples, the memory window increases with increasing the sweeping voltage. For each sweeping voltage, sample annealed at 800 °C has a larger memory window than that of the sample annealed at 875 °C. The smaller memory window of the 875 °C annealed sample is assumed to be due to two mechanisms. First, the SiO_2 tunnel oxide is thicker for the 875 °C annealed sample, and electrons are more difficult to transport through the tunnel oxide layer. Second, the concentration of oxygen vacancies, providing the defect energy levels for charge traps, will be further reduced under higher annealing temperature.

In the tri-layer structure CTF memory devices, the charge trapping mechanisms can be ascribed to the charges trapped in the quantum well, which is formed by the different band offsets of the block oxide, charge trapping oxide, and tunnel oxide. Yet for the present CTF memory devices with a MHOS structure, such a quantum well does not exist as there is no additional block oxide layer and thus cannot be the origin of the significant charge trapping effect. It has been reported that the HfO_2 film naturally has some intrinsic defects such as oxygen vacancies or interstitial oxygen atoms, which induces defect energy levels in the film.[20,21] These defect energy levels are believed to trap charges and to induce the large memory effects. To further investigate the features of the defect states in our electron-beam evaporation deposited HfO_2 films, PL and PLE measurements were carried out for the HfO_2 films annealed at 800 °C and 875 °C. The HfO_2 films were grown on fused silica substrates and the post deposition annealing processes were performed following the same procedure used in the MHOS structures. As shown in Fig. 3(a), the photoluminescence spectra under 325 nm excitation wavelength exhibit clear PL

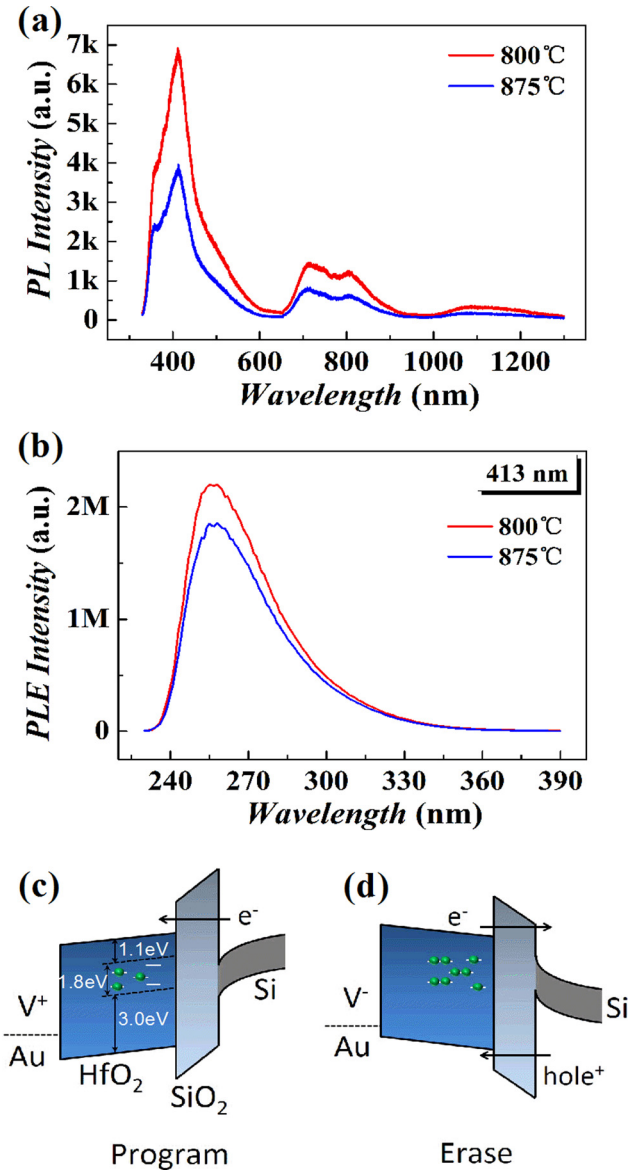

FIG. 3. (a) Photoluminescence spectra of HfO_2 films; (b) photoluminescence excitation spectra of the HfO_2 films by monitoring one of the PL peaks at 413 nm (3.0 eV); (c) a schematic diagram of the energy levels of the defect states and the programming process of the MHOS device; (d) a schematic diagram of the erasing process of the MHOS device.

peaks at 1.4–1.8 eV and at 2.1–3.5 eV for both of the two HfO_2 films. As the band gap of the HfO_2 film is around 5.9 eV,[20] the PL band at 1.4–1.8 eV and at 2.1–3.5 eV could not be due to the band-to-band recombination. Instead, it is most probably due to the recombination from defect states to valance band (E_V) or donor defect states to acceptor states, and thus clearly indicated the existence of the high concentration defects in the HfO_2 films. Furthermore, the sample annealed at 800 °C has a higher PL intensity than that of the sample annealed at 875 °C. If we consider that increasing the annealing temperature reduces the oxygen vacancy concentration in the HfO_2 films, then the PL results also imply that oxygen vacancies or interstitial oxygen atoms should be the dominant source for the defect states.

To further characterize the defect levels, the PLE spectra were measured by monitoring the strongest PL peaks at 413 nm (3.0 eV) of the two same HfO_2 films. With the

change of the excitation energy, the dominant photoluminescence peak appears at around 258 nm (4.8 eV) excitation energy for both of the two samples. Peaks in the PLE spectra also represent absorption lines of the material. Since the band-to-band absorption is not possible (the band gap of HfO_2 is around 5.9 eV[20]), the 4.8 eV peak in the PLE spectra represents the main defect states lying at 4.8 eV above E_V of the HfO_2 film. According to the theoretical simulations, the defect states mainly occupy the donor levels rather than the acceptor defect states in the HfO_2 film.[20,21,23] Therefore, the strongest PL peaks at 3.0 eV shown in Fig. 3(a) is assigned to the recombination processes from the donor states at 3.0 eV above E_V to the E_V of HfO_2 film. The electrons may first be excited to the defect states of 4.8 eV above E_V and then relaxed to the defect states of 3.0 eV above E_V without radiation. Finally, the relaxed electrons were recombined with the holes in the valence band with a luminance. Summarizing the PL and PLE results, we propose that the dominating defects lie at 4.8 eV above the valence band (that is 1.1 eV below the conduction band), and the defect states are relaxed down to the energy levels of 3.0 eV above the valence band (that is 2.9 eV below the conduction band). The energy level positions of the defect states are schematically shown in Fig. 3(c). Our experimental results on the energy levels of defect states in HfO_2 are highly consistent with the theoretical calculation results reported by Xiong *et al.*[20] and Perevalov *et al.*[21] In addition to the energy positions of the oxygen vacancies, the physical distribution of the oxygen vacancies was also investigated by the so-called constant current stress (CCS) method.[7] The charge trapping center (i.e., oxygen vacancy centre) is estimated to be 30 nm away from the metal/HfO_2 interface within the HfO_2 dielectric. Based on the PL and PLE analysis, the charge trapping and de-trapping processes can be schematically plotted, as shown in Figs. 3(c) and 3(d). Without fabricating quantum well in the MHOS device structures, the programming and erasing processes can be realized through the efficient charge transfers between the defect states and the silicon substrate.

Figure 4(a) shows the charge loss characteristics of the MHOS memory devices. The high and low capacitances are observed at a fixed read voltage of −1 V after a +10 V/1 s programming pulse or −10 V/1 s erasing pulse voltage. Excellent charge retention characteristics were observed for both the samples. For example, the high capacitance of 800 °C and 875 °C annealed devices only exhibit ~2.6% and ~1.5% charge loss after 10^4 s of retention. Especially, by extending the retention time to 10 yr by extrapolation, the high and low capacitance of 875 °C annealed sample can still maintain a large difference (as shown in the inset of Fig. 4(a) by using a log-scale of the retention time), indicating a strong charge confinement in the HfO_2 trapping layer. To further investigate the memory retention properties, the flat band voltage (V_{fb}) retention characteristics were also investigated. The V_{fb} values are extracted from the CV curves measured around flat-band voltage (within this voltage range, there will be no charge trapping and de-trapping process during the CV measurement). Figure 4(b) shows CV characteristics around V_{fb} of MHOS devices, indicating clear V_{fb} separation after programming and erasing voltage pulses. From the programmed/erased C-V characteristics by pulse

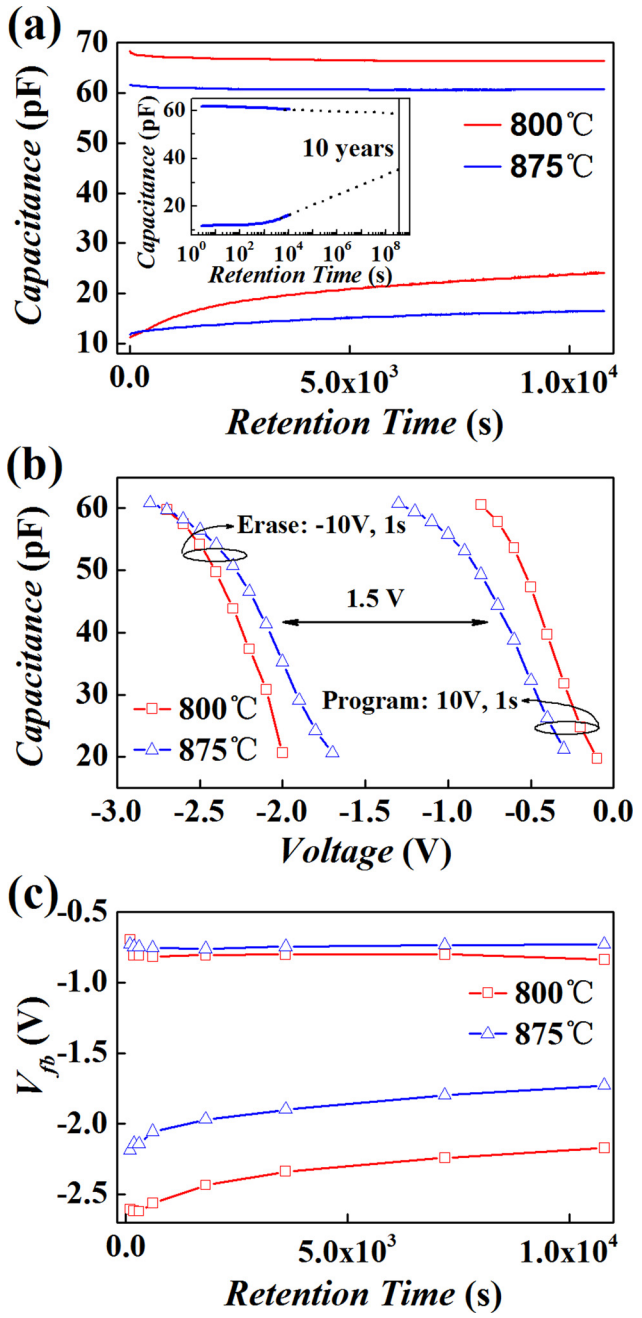

FIG. 4. (a) The long term retention characteristics of the high and low capacitances of the two MHOS devices, the inset shows the 10 yrs' retention extrapolating plot of the 875 °C annealed sample; (b) the C-V curves for V_{fb} measurement after programming/erasing processes; (c) the long term retention characteristics of V_{fb} of the two MHOS devices.

voltages, V_{fb} was measured with a time. Figure 4(c) shows the excellent V_{fb} retention characteristics for both of the memory devices. Except for the fast decay in the first several minutes, the V_{fb} values remain very stable even after more than 10^4 s retention. It should be mentioned that the sample without any annealing exhibits much worse retention compared to that of the 800 °C and 875 °C sample (results not shown), which implies that the SiO_2 formed during the annealing plays an important role on preventing the charge tunneling back to the Si substrate. The detailed mechanisms will be discussed in the following text.

The excellent charge trapping characteristics of our MHOS devices are believed to originate from the high density

of deep defect states of HfO_2 films deposited by electron beam deposition. The HfO_2 films were deposited by electron beam evaporation in a high vacuum ($\sim 4.0 \times 10^{-4}$ Pa), and it can provide a huge amount of oxygen vacancy defects for charge trapping. By using a simple calculation method, the charge trapping density can be estimated as[22] $N_{charge} = \Delta V_{fb} \times C_{ox}$, where C_{ox} is the total oxide capacitance per unit. For the 875 °C annealed HfO_2 films, the calculated charge trap density was $\sim 4.1 \times 10^{12}\,cm^{-2}$, and the memory window of the corresponding MHOS device was 3.2 V under ±10 V sweeping voltages. When the annealing temperature changed to 800 °C, a higher charge trap density of $\sim 7.5 \times 10^{12}\,cm^{-2}$ has been observed, which produced a larger memory window of ~5.1 V. The calculated values of the charge trap density in our experiment are very close to the values reported by Maikap *et al.*[22] ($\sim 1.1 \times 10^{13}/cm^2$) and Chen *et al.*[24] ($6.4 \times 10^{12}/cm^2$). These results indicate that the electron-beam evaporation deposited HfO_2 film can provide a high density of charge traps, and the density can be controlled by a simple annealing process. The excellent charge retention properties of the present MHOS devices are attributed to two mechanisms. The first and most critical mechanism is assumed to be the deep defect states for charge confinement of the trapped charges. As analyzed from the PL and PLE studies shown in Fig. 3(c), the defect states in the HfO_2 films distributed in deep energy levels ranging from 1.1 eV to 2.9 eV below the conduction band, which provide high potential barriers for the trapped charges to tunnel back to the silicon substrate. The second mechanism is assumed to be the large conduction band offset between HfO_2 charge trapping layer and the SiO_2 tunneling layer. According to Robertson's work, the band offset between most of the high-*k* oxide is less than 2 eV.[25] For example, the reported band offset for Al_2O_3/HfO_2/Al_2O_3 fabricated by atomic layer deposition (ALD) is only 1.48 eV.[5] In the present MHOS devices, the conduction band offset between the HfO_2 charge trapping layer and the SiO_2 tunneling layer is as large as 2 eV,[25] which provides much deeper charge barriers than those provided by the conventional tri-layer high-*k* oxide based CTF memory devices.

In summary, we have correlatively investigated the charge trapping characteristics and the defect states of the electron-beam-evaporation deposited high-*k* HfO_2 films. The MHOS device structure can be easily constructed by annealing the HfO_2 films at high temperature, and the thickness of the SiO_2 tunnel oxide can be controlled by changing the annealing temperature. The significant memory effects demonstrated in the Au-HfO_2-SiO_2-Si devices are attributed to the oxygen vacancies induced defect energy levels in the HfO_2 films, as revealed by PL measurements. Moreover, the MHOS devices exhibit excellent long-term retention properties. Our results demonstrated that the HfO_2 based MHOS memory device is promising for future flash memory applications.

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