All-Optical Bit-Error Monitoring System Using Cascaded Inverted Wavelength Converter and Optical NOR Gate

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Abstract—A novel all-optical bit-error monitoring system is demonstrated by cascading two all-optical logic gates: an inverted wavelength converter and an optical NOR gate which are realized using injection-locked laser diodes operating at different thresholds. Real-time optical monitoring signal is generated which indicates the positions and duration of both bit and burst errors in 10-Gb/s nonreturn-to-zero signals.

Index Terms—Bit-error monitoring, injection locking, optical data processing, optical logic gate.

I. INTRODUCTION

REAL-TIME bit-error monitoring of high-speed optical transmission is crucial for fault management [1], quality of service, optical layer protection [2], and eye monitoring for adaptive polarization-mode dispersion (PMD) compensation [3] in high capacity transport and access networks. Typical error monitoring schemes require expensive optical–electrical conversions and high speed large-scale integration chips [4]. Real-time all-optical bit-error monitoring is useful for future all-optical networks as the generated optical error signals can be forwarded to the corresponding network node for processing using the same network. It is, however, difficult to implement a real-time error-monitoring system all-optically because of the limited signal processing capabilities of current all-optical devices. In this letter, we demonstrate, to the best of our knowledge, the first real-time all-optical bit-error monitoring system (BEMS) at 10 Gb/s using two multiwavelength mutual injection-locked Fabry–Pérot laser diodes (FP-LDs) without employing any high speed electronics. Relatively complex logic operations, two threshold, one NOT, and one NOR, functions are realized. The proposed BEMS uses two threshold levels to determine the error bits. The resulting optical indicator signal,

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K. K. Qureshi and H. Y. Tam are with the Photonics Research Center, The Hong Kong Polytechnic University, Kowloon, Hong Kong, and also with the Department of Electrical Engineering, The Hong Kong Polytechnic University, Kowloon, Hong Kong.

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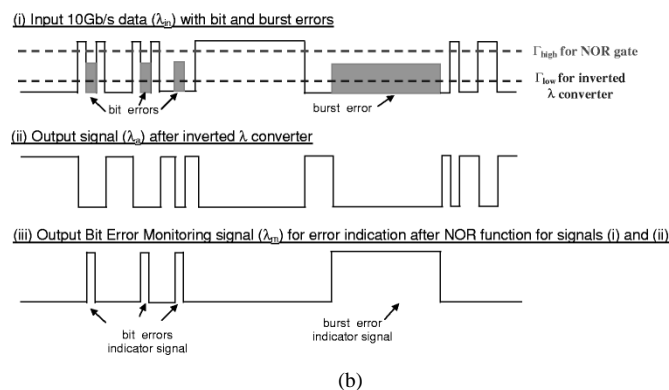| p	Inverted λ converter (NOT gate)		Optical NOR Gate	
	$TH_1(p)$	$NOT[TH_1(p)]$	$TH_2(p)$	$NOR\{NOT[TH_1(p)], TH_2(p)\}$
1	1	0	1	0
E	1	0	0	1
0	0	1	0	0

(a)

(b)

Fig. 1. (a) Truth table of the logical function $NOR\{NOT[TH_1(p)], TH_2(p)\}$ implemented by the BEMS. The input p takes on values 0, 1, and E where $0 < E < 1$ represents an error bit. (b) Basic principle of all-optical BEMS. (i) A 10-Gb/s input signal with the error bits in grey. (ii) The ideal inverted wavelength converter output. (iii) The ideal output of the BEMS.
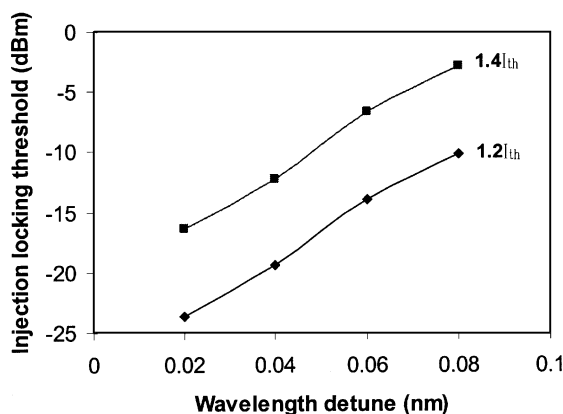

Fig. 2. Injection locking threshold versus wavelength detunes for two different FP-LD biasing currents. (Note: I_{th} = threshold current of FP-LD).

sometimes known as the "pseudoerror" signal, identifies both the positions and the durations of the error bits and can be used in performance monitoring such as eye monitoring [3].
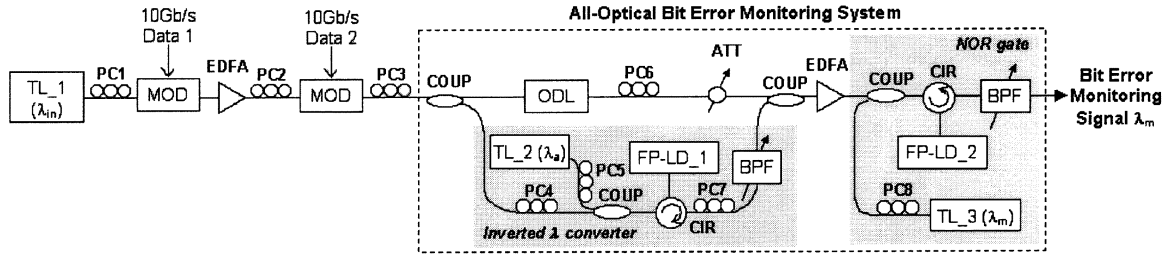
Fig. 3.   Experimental setup for the BEMS. Note: PC—polarization controller; MOD—modulator; COUP—coupler; ODL—optical delay line; ATT—variable attenuator; CIR—circulator; and BPF—tunable bandpass filter.

II. OPERATION PRINCIPLES

The all-optical bit-error monitoring system is realized using two stages of all-optical processes: a NOT gate to perform an inverted wavelength conversion of the input signal and a NOR operation for the wavelength converted NOT gate output signal and the original input signal. In the proposed scheme, we identify an error using two optical threshold levels Γ_{low} and Γ_{high}, where $\Gamma_{\text{high}} > \Gamma_{\text{low}}$ [Fig. 1(b)], instead of just one decision level in conventional electronic bit-error test sets. If the optical intensity in a bit period is above Γ_{high} (below Γ_{low}), the bit period is assumed to contain a correct "1" ("0") bit. If the optical intensity falls in between the two threshold levels, the bit period is assumed to contain an error bit. Thus, the data bit p in any signal can be classified to be in one of the three states, 0, 1, or E, where state E represents an error bit of value between 0 and 1. The operation of the BEMS can be realized using the logic operation NOR$\{$NOT$[\text{TH}_1(p)], \text{TH}_2(p)\}$, where TH_1 and TH_2 are threshold decision functions using the logical threshold levels γ_{low} and γ_{high}, respectively. The γ_x is the logical value corresponding to the optical intensity Γ_x where $x = \text{low, high}$ and $0 < \gamma_{\text{low}} < \gamma_{\text{high}} < 1$. That is, $\text{TH}_i(p) = 1$ if $p \geq \gamma_x$ and $\text{TH}_i(p) = 0$ if $p < \gamma_x$ where $i = 1, 2$, and $x = \text{low, high}$. The logical threshold levels are chosen such that $\gamma_{\text{low}} < E < \gamma_{\text{high}}$. These two logical threshold levels, γ_{low} and γ_{high}, correspond to the operation thresholds for the inverted wavelength converter (Γ_{low}) and optical NOR gate (Γ_{high}), respectively. Fig. 1(a) shows the truth table of the logic operation, NOR$\{$NOT$[\text{TH}_1(p)], \text{TH}_2(p)\}$ by the BEMS. The basic principles for the BEMS are illustrated in Fig. 1(b). Fig. 1(b-i) shows a 10-Gb/s data signal at wavelength λ_{in}. The shaded bits identify both bit and burst errors. The 10-Gb/s corrupted data is then split into two portions, one of which undergoes inverted wavelength conversion and the other portion remains unchanged. Fig. 1(b-ii) shows the output of the inverted wavelength converter, i.e., the NOT gate, which performs the logic functions NOT$[\text{TH}_1(p)]$. The wavelength converted signal in λ_a is then combined synchronously with the unmodified portion of the original corrupted 10-Gb/s signal in λ_{in} and fed into the optical NOR gate as shown in Fig. 1(b-iii). After the NOR operation, the output signal in λ_m identifies the position and duration of the error bits. The nature of the errors, bit or burst, are given by the duration of the output signal. In the experiment, the BEMS was realized using two injection-locked FP-LDs which functioned as the inverted wavelength converter and the optical NOR gate. The decision thresholds (Γ_{high} and Γ_{low}) can be tuned by varying the wavelength detunes (the wavelength differences between the

signal and the FP longitudinal modes) and the bias current of the FP-LDs (Fig. 2).

III. EXPERIMENTAL RESULTS

Fig. 3 shows the schematic of the experimental setup to demonstrate the all-optical BEMS. The corrupted 10-Gb/s nonreturn-to-zero (NRZ) data signal was generated using two 10-Gb/s modulators on the output of a tunable laser (TL_1). Data 1 and Data 2 are the two 10-Gb/s data sequences that fed into the two modulators. Data 2 is a delayed copy of the complement of Data 1. By operating the modulators at different extinction ratios, we could vary the intensities of individual bits. The bits with intensities between the two threshold levels were considered as error bits. We introduced both single-bit errors and burst errors. Thus, the errors in the corrupted signal are due to amplitude jitters only. We did not consider other sources of signal degradation such as signal-to-noise ratio degradation and waveform deformation. We then split the corrupted signals into two parts. One part was injected into an FP-LD (FP-LD_1) which functioned as an inverted wavelength converter. FP-LD_1 implemented the operation of TH_1 and the NOT gate using dual wavelength mutual injection locking [5]. Besides the input 1542.67-nm (λ_{in}) 10-Gb/s data signal, we also injected a continuous-wave (CW) signal at 1548.32 nm (λ_a) into FP-LD_1. The 10-Gb/s data and the CW signal were wavelength detuned from two different longitudinal modes of FP-LD_1 at the longer wavelength side with values of 0.18 and 0.06 nm, respectively. The biasing current of FP-LD_1 is 1.3 $I_{\text{th\_1}}$ where $I_{\text{th\_1}}$ is the threshold current of FP-LD_1. The threshold level for FP-LD_1 was set to Γ_{low} such that an error bit in the data signal was treated as a "1." The powers of the data and CW signals were chosen such that a "1" bit or an error bit in the data signal would injection lock FP-LD_1. Thus, the inverted data signal obtained at 1548.32 nm in the output of FP-LD_1 had all the error bits converted to zeroes.

The other part of the original 10-Gb/s corrupted data signal was injected into another FP-LD (FP-LD_2) together with the 1548.32-nm output from FP-LD_1 which was synchronized to the 10-Gb/s data signal by the variable delay line (ODL). We also injected a CW signal at 1546.11 nm (λ_m) into FP-LD_2. FP-LD_2 realized the logic operations TH_2 and the NOR gate using multiwavelength injection locking. The biasing current of FP-LD_2 is 1.1 $I_{\text{th\_2}}$ where $I_{\text{th\_2}}$ is the threshold current of FP-LD_2. Note that because the overall injected powers into FP-LD_2 is smaller than that of FP-LD_1, the biasing current
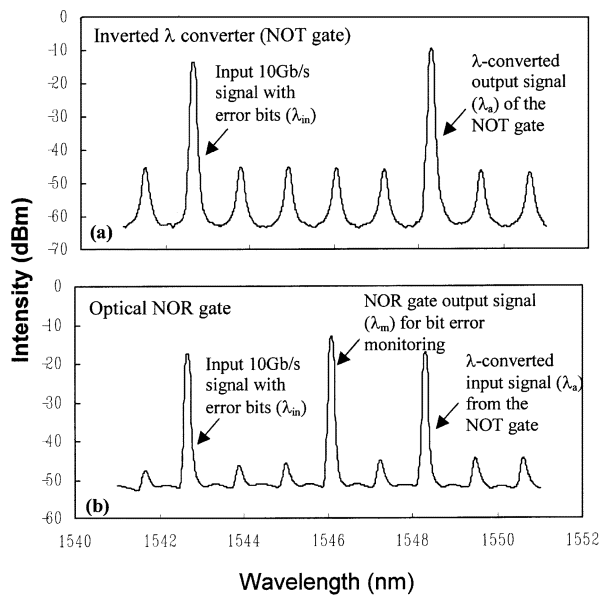
Fig. 4. Output spectra of (a) the inverted wavelength converter (FP-LD_1) and (b) the optical NOR gate (FP-LD_2) under injection locking in BEMS.

Fig. 5. Synchronized temporal profiles of (a) the input 10-Gb/s NRZ signals at 1542.67 nm with both bit and burst errors, (b) the inverted λ-converted signal at 1548.32 nm, and (c) the error indicator signals generated by the BEMS at 1546.11 nm.

required for FP-LD_2 (1.1 $I_{\text{th\_2}}$) to set a high threshold (Γ_{high}) is smaller than the biasing current for FP-LD_1 (1.3 $I_{\text{th\_1}}$) to set a low threshold (Γ_{low}). The threshold level for FP-LD_2 was set such that an error bit in the data was treated as a "0." The powers and detunes (wavelength differences between the signals and the respective FP-LD longitudinal modes) of the three inputs to FP-LD_2 were chosen such that the 1546.11-nm CW beam injection locked FP-LD_2 only when both the data signal and the FP-LD_1 output were low, i.e., zeroes. The incident powers for λ_{in}, λ_a, and λ_m at the NOR gate were 1.43, 0.3, and -3.13 dBm, respectively. Consequently, the "1" bits at 1546.11 nm in the output of FP-LD_2 indicated both the position and duration of any errors in the original signal.

Fig. 4(a) and (b) shows the spectra of the NOT gate (FP-LD_1) and the NOR gate (FP-LP_2) output, respectively. Fig. 5 summaries the operation of the BEMS. Fig. 5(a) depicts the 10-Gb/s corrupted NRZ signal. The solid arrows identify single bit errors while the open arrows identify burst errors. Fig. 5(b) shows the inverted and wavelength converted data output signal of FP-LD_1 at 1548.32 nm. Note that all the error bits in the original signals are now converted to zeroes. Fig. 5(c) gives FP-LD_2 output at 1546.11 nm. All the error bits in the original signals now appear as "1" bits. The proposed scheme is sensitive to the polarization of the input signals because the scheme utilizes the injection-locking mechanism in FP-LD. Previous experiments show that an injecton-locked FP-LD is both wavelength and power stable; we observe wavelength and power fluctuations of less than 0.01 nm and 0.5 dB, respectively, in a three-day continuous operation with simple feedback control.

IV. CONCLUSION AND DISCUSSIONS

We have successfully demonstrated all-optical error monitoring at 10 Gb/s using two mutual injection-locked FP-LDs. Relatively complex l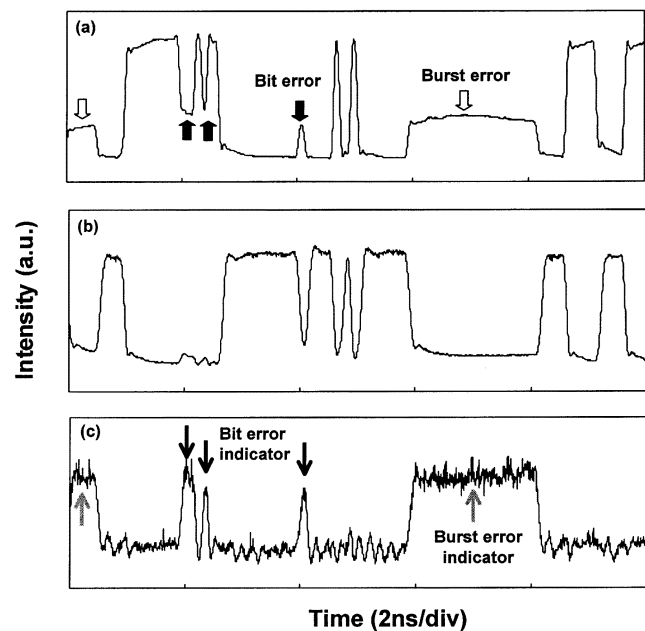ogic operations, two threshold, one NOT, and one NOR functions, were realized all-optically. Since the FP-LDs allow different wavelengths for input and output signals, only one physical path is required for the input signal. The proposed scheme can be tailored to monitor the system with any specific BER because one can tune the threshold levels of the two optical logic gates by varying the biasing currents, wavelength detunes and the powers of the signal injected into the FP-LD. In this work, we use two commercially available FP-LDs to achieve error monitoring at 10 Gb/s. High-speed monitoring systems at 40 Gb/s and beyond should be possible by replacing the FP-LDs with high-speed multiple quantum-well FP-LDs [6].

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