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A Novel Single-Phase Voltage Sag Restorer with Diode-Clamped Multilevel Bridge

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Abstract — A novel single-phase voltage sag restorer with diode-clamped multilevel bridge is presented. In the proposed circuit, traditional two-level half bridge inverter is replaced by multilevel diode-clamped inverter, in which the dc-bus voltage is split into several levels by series-connected bulk capacitors. Although the multilevel circuit has more component count than the two-level circuit it is more suitable for high voltage applications. The restorer is bypassed under normal operating conditions and is connected to the load depending upon voltage sag detection. The switches of the inverter are controlled by PWM signals. In the paper the operation of the multilevel circuit is simulated in SABER to study the operating capability of the multilevel inverter. A comparative study between the traditional two-level circuit and the proposed multilevel circuit is provided to highlight the performance of the multilevel circuit.

Keywords — Voltage sag, Power interruption, Power system, Diode-Clamped, Multilevel

I. INTRODUCTION

Power interruptions have become rare events with the improvement of reliability and availability of the power system [1,2]. However, voltage sags are the most common power disturbance and probably the most significant power quality problem [2-14]. The voltage sags are caused by faults on adjacent lines or starting of motors. The non-zero impedance of a Power grid causes voltage drop at the point where the load is connected. Usually, these drops are very small such that the voltage remains within normal ranges [15]. But under heavy load condition where there is a large increase in current, or when the impedance of the system is high, a significant voltage drop may occur. Such voltage variations are not desirable for sensitive loads [8,16]. Voltage sags are defined as a decrease in root mean square (rms) voltage at the power frequency. Voltage sag is not a complete interruption of power but a momentary drop in the magnitude of the voltage. It is a temporary drop below 90 percent of the nominal voltage level. Most voltage sags do not go below 50 percent of the nominal voltage, and they normally last from 3 to 10 cycles—or 50 to 170 milliseconds [3]. Sags do not generally disturb incandescent or fluorescent lighting, motors, or heaters. However, some electronic equipment lacks sufficient internal energy storage and, therefore, cannot ride through sags in the supply voltage [15].

Various solutions have been proposed to mitigate sags, examples being: Designing inverter drives for process equipment to be more tolerant of voltage fluctuations or the installation of voltage correction devices. For certain end users of sensitive equipment the voltage correction device may be the only cost-effective option available. It has already been shown that for customers of large loads, from the high kilowatt to the low megawatt range, a good solution is the installation of a dynamic voltage restorer (DVR)[17]. DVR is one of the custom power devices capable of protecting sensitive loads from all supply-side disturbances. Numerous circuit topologies and methods are available for DVR [2, 5, 6, 8,-11, 13, 17-36]. The main limitation of some of the solutions is the use of 50 Hz interfacing transformer. As a result the power electronics circuits are limited in application by presence of low frequency transformer, which must be able to handle full rated power [37]. In order to address this issue, dynamic voltage sag corrector s(DySC) without an interfacing transformer are proposed[32, 37, 38]. The topology is derived from a voltage boost circuit and is small in size and weight. The standard DySC products, up to 500-kVA modules, do not include a series transformer, and include little energy storage.

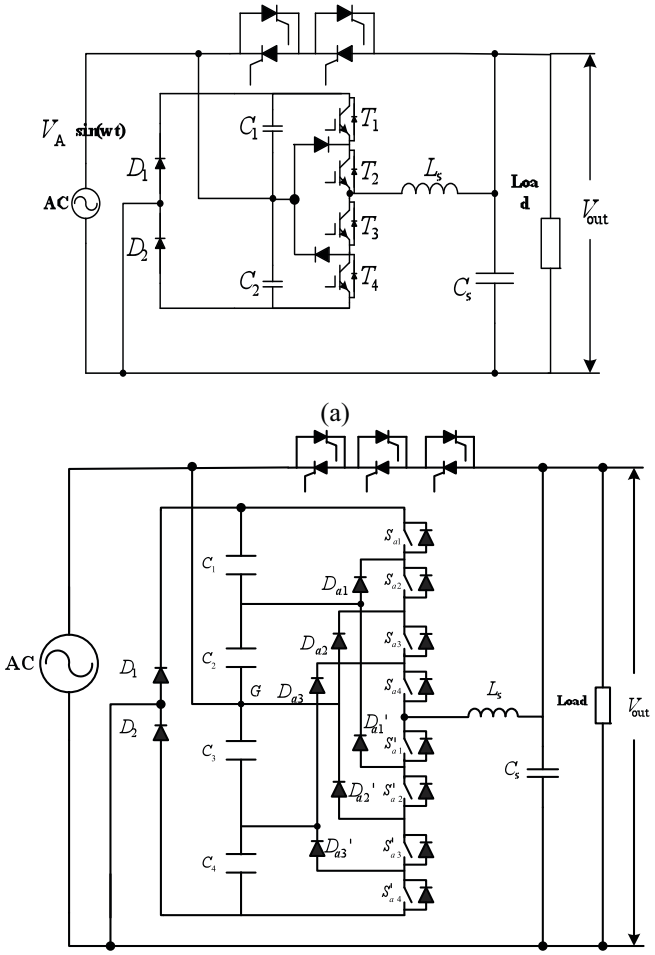

Fig. 1. Single-phase voltage sag restorer with multilevel diode-clamped bridge (a) Three-level (b) Five-level circuit

For high voltage application, the switches with high voltage rating have to be used in such circuits. In this paper, a

single-phase voltage sag restorer with multilevel diode-clamped bridge is proposed by which the circuit can be used at high voltage but with switches of low voltage rating. Subharmonic PWM modulation method used for multilevel converters is employed for controlling the power switches in the circuit. Simulation results are provided to validate the feasibility of the proposed concept.

The diode-clamped multilevel bridge inverter circuit is discussed in II, operation of the voltage sag restorer is presented in III, simulation results are given in IV followed by conclusion.

II. DIODE-CLAMPED MULTILEVEL BRIDGE

A. Diode-Clamped multilevel converter

Fig. 2 shows a schematic of a single phase Diode-clamped multilevel converter. In general, the output voltage of a given multilevel converter can be calculated from (1) as:

$$V_o = (S - \frac{n-1}{2})E \qquad (1)$$

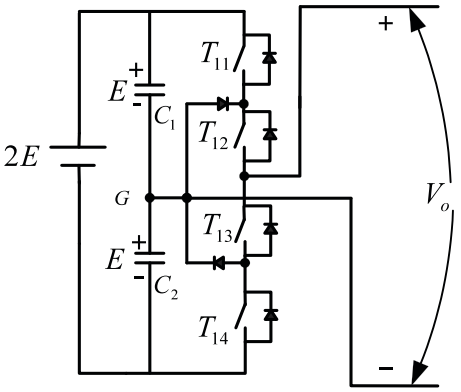

Figure 2 Diode-clamp multilevel bridge

Where V_0 is the output voltage of the multilevel converter, n is the number of the output levels; S is the switching state that ranges from 0 to n-1. E is the minimum voltage level the multilevel converter can generate.

Assuming the DC bus voltage of the converter is 2E, it can be easily found from Figure 2, that when T_{11} ,T_{12} are on T_{13} ,T_{14} are off or T_{12} ,T_{13} are on T_{11} ,T_{11} and T_{14} are off or T_{11} ,T_{12} off T_{13} ,T_{14} on, the output voltage of V_o is +E, 0, -E, respectively. So the "S" ranges from 0, 1, 2 and three voltage levels can be synthesized.

B. Subhamonic PWM method

Subhamonic PWM is a conventional control method suitable for multilevel converter. The control principle of the SHPWM method is to compare several triangular carrier signals with only one sinusoidal reference signal per phase. For example, in an n-level inverter, n-1 triangular carrier signals of the same frequency f_c and the same peak-to peak amplitude A_c, are disposed such that the bands they occupy are contiguous.

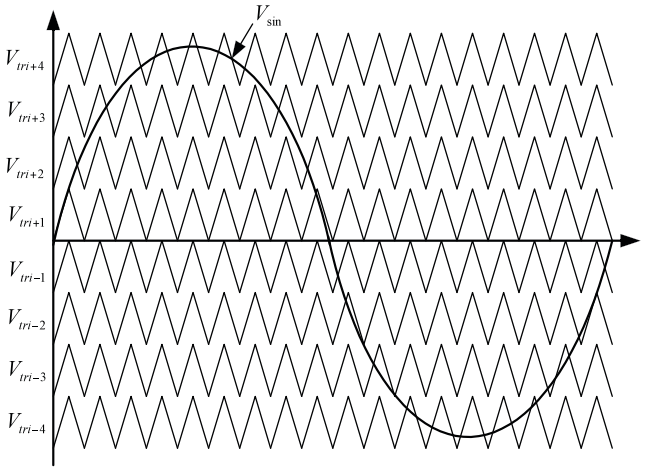

Figure 3 Principle of Subhamonic PWM method.

The zero reference is placed in the middle of the carrier set. The modulation wave is a sinusoid of frequency f_m and amplitude A_m. At every instant, each carrier is compared with the modulation waveform generating the gating signal for the switches in the respective levels. Comparison of the respective triangular signals with the sine signal results in switching on of the devices if the reference signal is greater than the triangular carrier assigned to that device level; otherwise, the device is turned off. For example, in a nine-level inverter shown in Fig. 4, eight triangular carriers are compared with a sinusoid modulation waveform as shown in Figure 3. Whenever $V_{sin}>V_{tri+4}$ the switching state S is 8 resulting in an output voltage of V_{ac} equal to +4E， and whenever $V_{tri+4}>V_{sin}>V_{tri+3,}$ the switching state S is 7 resulting inV_{ac} equal to +3E and so on. On the other hand when $V_{sin}<V_{tri-4}$, the switching state S is 0 and the output voltage V_{ac} is -4E. Thus different switching combination can be selected according to the switching state "S"to generate different voltage levels.

III. VOLTAGE SAG RESTORER WITH MULTILEVEL DIODE-CLAMPED BRIDGE

The voltage sag restorer proposed here is similar to the conventional voltage sag restorer but for the use of multilevel half-bridge diode-clamped inverter. As shown in Fig. 1, the single phase voltage sag restorer is derived from voltage doubler[20, 32, 33, 37, 38] and a half-bridge multilevel diode-clamped inverter. The inverter is configurable to work in voltage boost or bypass mode, and is capable of providing 100% step-up to the ac grid voltage. Under normal working conditions, the anti-parallel SCRs are closed, and a normal line voltage is provided directly from the input line. When any voltage sag is detected, the SCRs are opened and the multilevel inverter bridge is controlled to resurrect the voltage to the load.

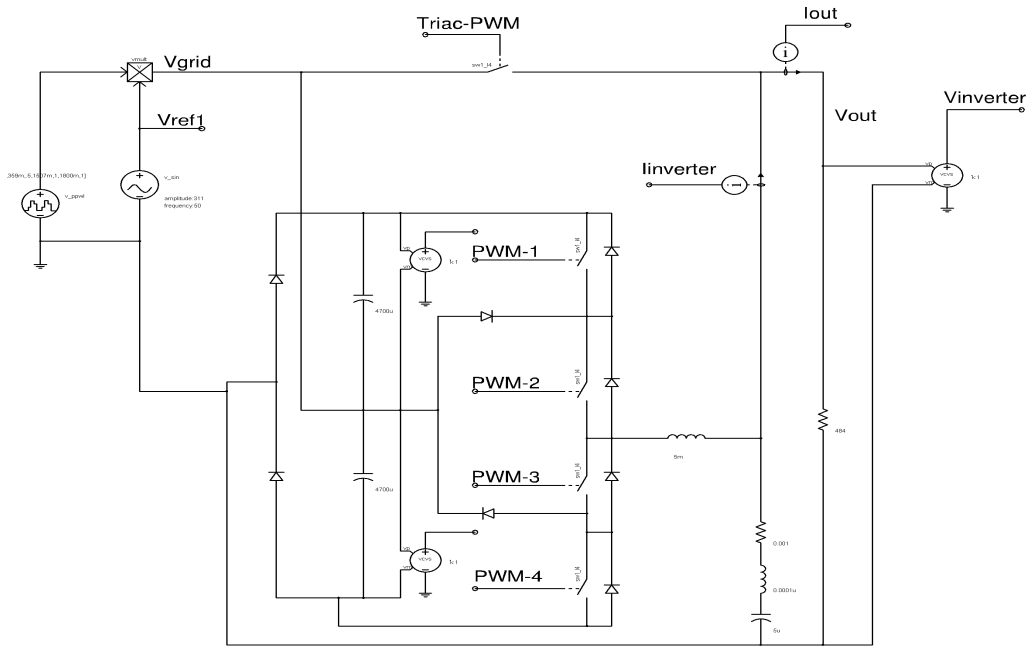

Figure 4: Schematic of the main circuit of the proposed system

IV. Simulation Verification

The proposed DVR system based on three-level diode-clamped inverter bridge is simulated using the SABER program for a 2kVA load to verify the effectiveness of the proposed technique. A simulation of the system shown in figure 1(a) is carried out. The schematic of the model is shown in figure 4 and the control circuit is shown in figure 5. The voltage sag detection is implemented in the RMS voltage detection block as in figure 6.

The main parameters used in the simulation are given as: C_1= C_2=4700uF, L_s=5mH C_s=10uF and the switching frequency f_s is 10 kHz. Figure 7 illustrates the voltage restoration performances of the three levels DVR system during source-side single-phase voltage sag. Measured three-level PWM output voltage and inverter output are shown in Figure 8. The measured driving signals and DC-link capacitor voltage are shown in
Figure 9 and Figure 10 respectively.

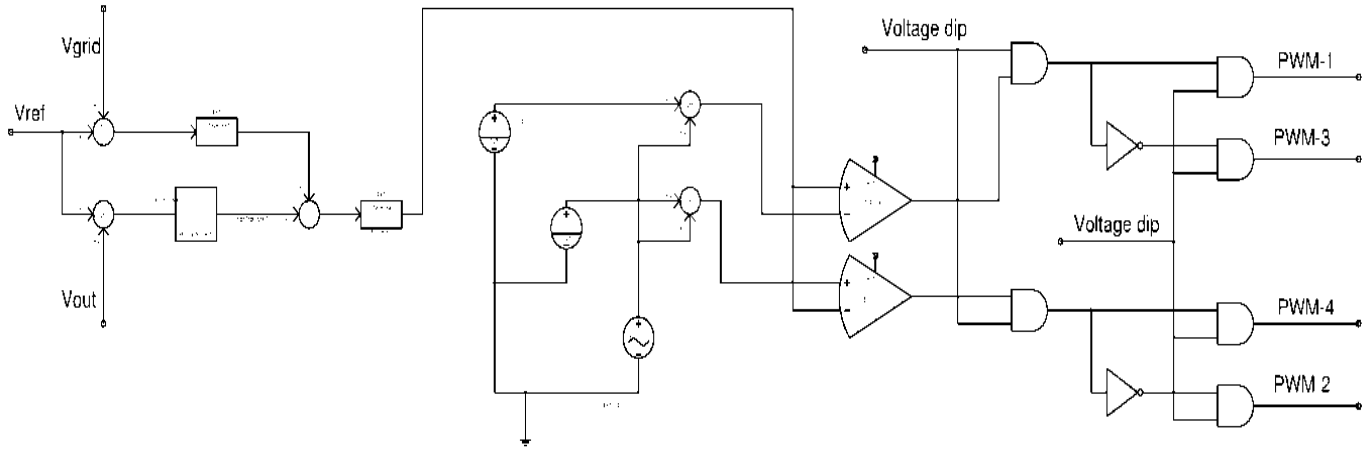

Figure 5: Schematic of the control circuit of the proposed system

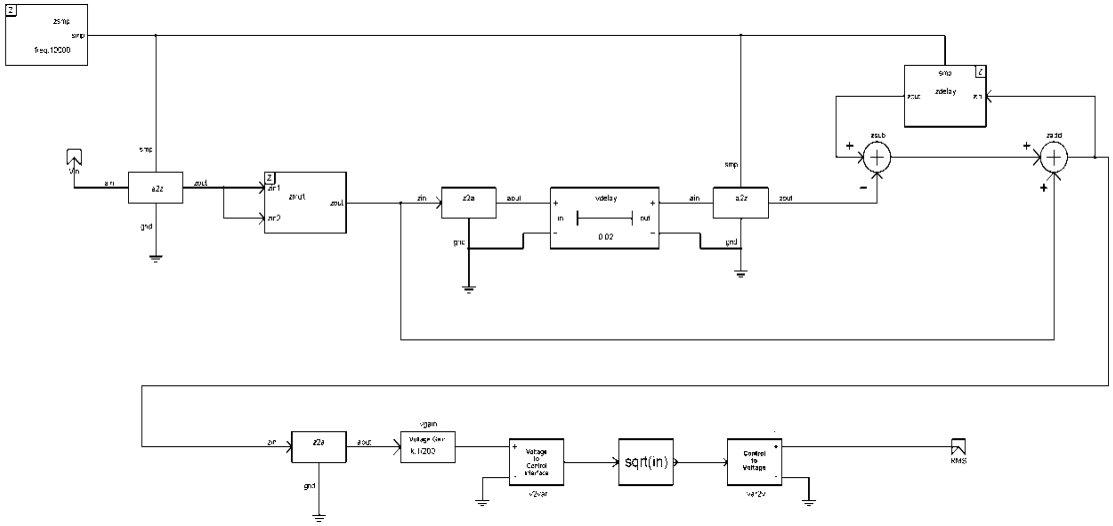

Figure 6: Schematic of RMS voltage detection block

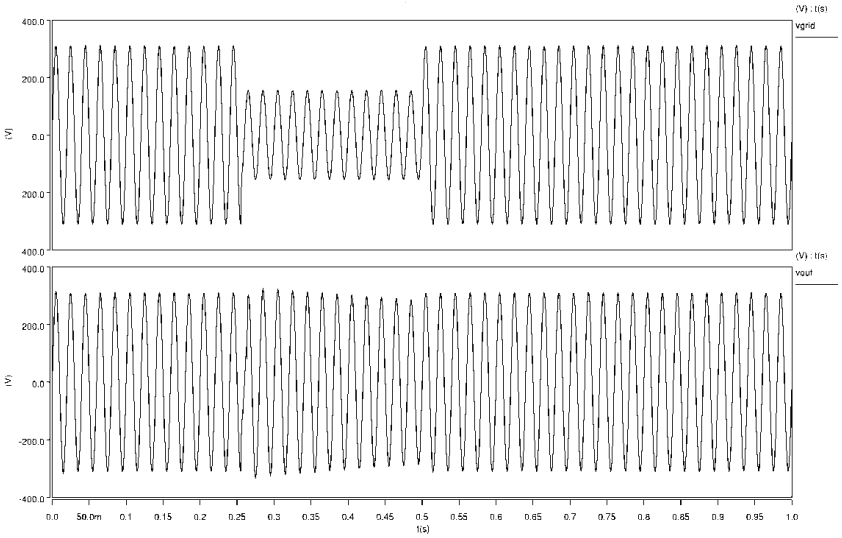

Figure 7: Measured source-side single-phase voltage and the output voltage across load (2kVA). Upper: source-side single-phase voltage, vgrid; Lower: output voltage, vout.

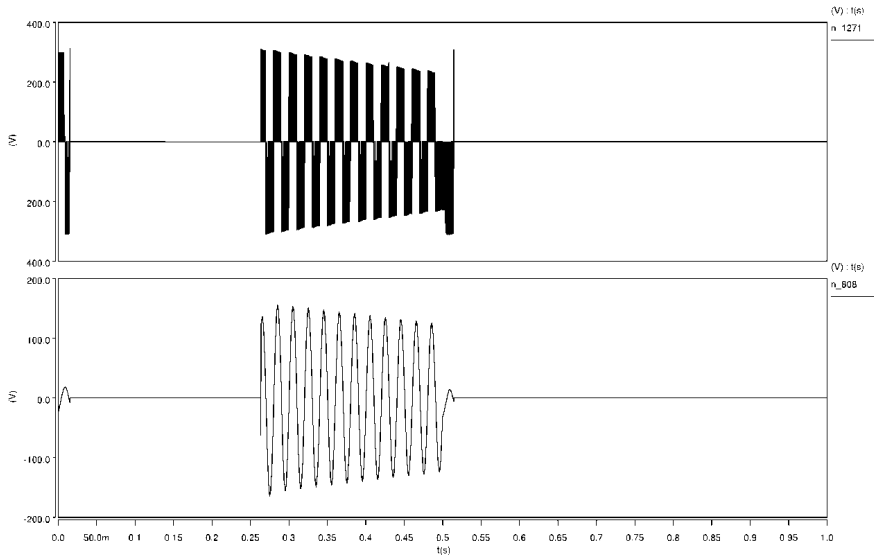

Figure 8: Measured three-level PWM voltage and inverter output voltage. Upper: inverter three-level PWM voltage; Lower: inverter output voltage.

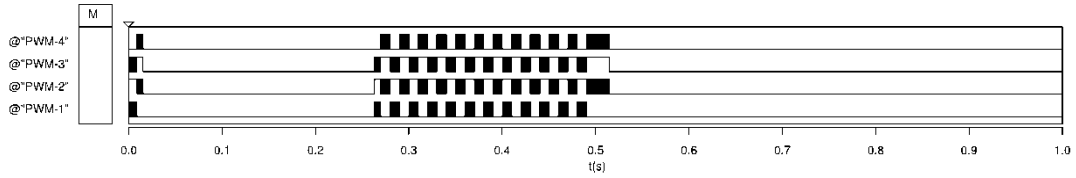

Figure 9: Measured gate driving signals of switches in diode-clamped inverter bridge, PWM1~PWM4.

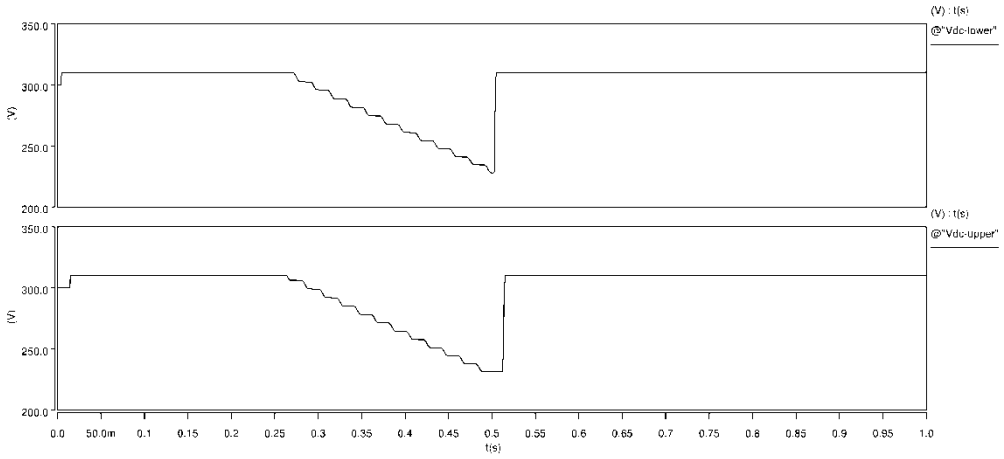

Figure 10: Measured Dc-link capacitor voltage.
Upper: DC voltage across lower capacitor; lower: DC voltage across upper capacitor

V. CONCLUSION

A multilevel diode-clamped inverter based DVR system is proposed in this work. In the circuit, the dc-bus voltage is split into several levels by series-connected bulk capacitors with neutral at the mid point. The advantages of the proposed topology when compared with two-level topology are: 1) Voltage stress across IGBT is reduced by half; 2) it can result in higher voltage levels 3) Resulting in smaller size filter due to reduced harmonic content 4) Suitable for high voltage application with lower rating switches such as for 10kV power transmission line. The disadvantages of the proposed topology are: 1). Higher component count 2) Complex control and large package layout.

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