

MATERIALS SCIENCE

Surface proximity effect enables layer-by-layer growth of MoS₂

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Two-dimensional (2D) monolayer semiconductors have shown great potential for continuous downward scaling to a 2-nm technology node [1]. However, the monolayer characteristics make it quite challenging to completely manifest their intrinsic high performance. At the interface between semiconductors and dielectrics, the carriers are scattered by extrinsic impurities and remote optical phonons, which seriously degrade their carrier mobility; at the electrical contact, the relatively wide band gap of monolayer MoS₂ hinders efficient carrier injection. Few-layer (bilayer or trilayer) MoS₂ have been suggested with higher mobility and lower contact resistance, and can still retain excellent electrostatic control at sub-5-nm nodes [2]. However, precise control of growing wafer-scale bilayer or trilayer MoS₂ remains a grand challenge from a thermodynamic perspective.

According to the criteria defined by E. Bauer and J.H. van der Merwe [3], the 2D growth mode requires that the substrate surface energy (γ_s) is larger than the sum of freestanding MoS₂ surface energy (γ_o) and the MoS₂/substrate interface energy (γ_i), i.e. $\gamma_s > \gamma_o + \gamma_i$. The surface energy of freestanding MoS₂ increases with the number of layers, which results in the self-limiting characteristics of monolayer MoS₂ growth. Different from the very recent edge-aligned bilayer strategy [4], Zhang and his colleagues analyze the surface proximity effect and successfully demonstrate controllable growth of wafer-scale bilayer and trilayer MoS₂ in a layer-by-layer mode, by optimizing both thermodynamic and kinetic factors (Fig. 1a and b) [5].

Thermodynamically, they adopt sapphire (0001) with very high substrate surface energy ($\sim 3.3 \text{ J/m}^2$). By analyzing the energy relationship of MoS₂/sapphire as a new substrate, they identify that it is still energetically feasible to grow additional MoS₂ layers on monolayer and bilayer MoS₂/sapphire substrate. This surface proximity effect enables the growth of bilayer and trilayer MoS₂ in a layer-by-layer manner on

MoS₂/sapphire substrate with relatively high surface energy. With the increase of the layer number, the growth mode evolves from 2D to 3D because of the weakened proximity effect, which makes it thermodynamically unfavorable for growing thicker MoS₂.

To achieve full coverage and a controlled layer number, researchers are also required to optimize kinetic growth factors. They increase Mo-source flux with

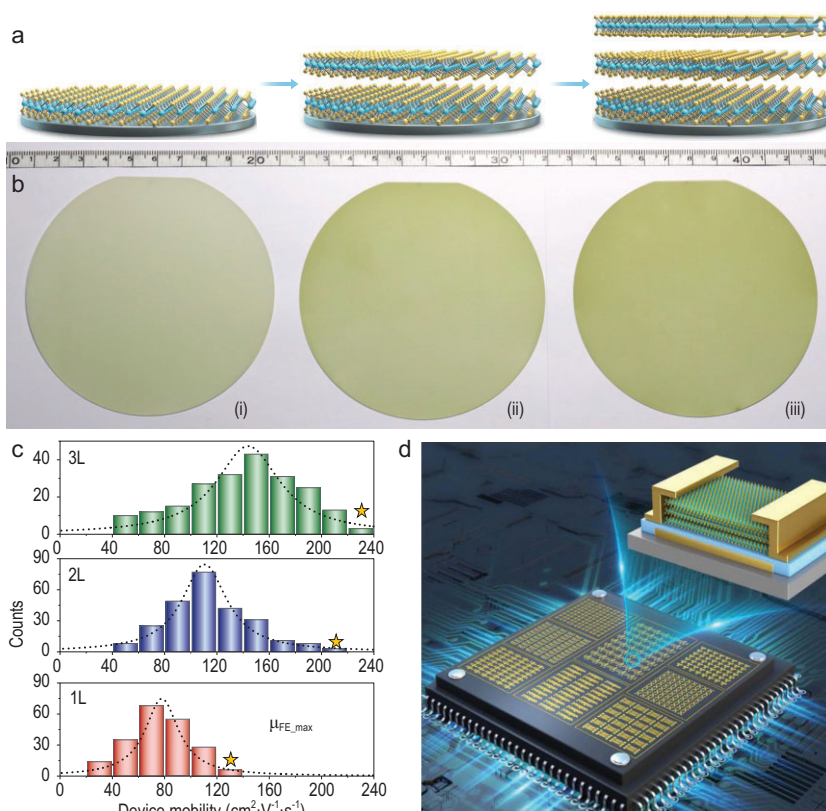


Figure 1. (a) Schematic illustration of the layer-by-layer growth process [5]. (b) Photographs of 4-inch (i) monolayer, (ii) bilayer and (iii) trilayer MoS₂ wafers [5]. (c) Statistical distribution of the field-effect mobility of mono-, bi- and trilayer MoS₂. The stars indicate the maximum values achieved in each type of device [5]. (d) Prospect of integrated logic circuits based on thicker-layer MoS₂ wafers.

high source temperature for high nucleation density on the substrate. By adopting oxygen-assisted chemical vapor deposition, they also achieve ultra-high edge growth rate ($\sim 5\text{--}10\ \mu\text{m}/\text{min}$) compared to that without the oxygen assistance ($< 0.1\ \mu\text{m}/\text{min}$). With the optimization of the nucleation density and the edge growth rate, the diffusion mean free path is larger than the domain size, allowing uniform layer-by-layer growth at a wafer scale (Fig. 1b).

Furthermore, they fabricate long- and short-channel field-effect transistors using mono-, bi- and trilayer MoS_2 . Thick-layer field-effect transistors produce significant improvements in device performance. For long-channel devices (channel length of 5 to 50 μm), the average field-effect mobility is

$\sim 80\ \text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$ for monolayers, to $\sim 110/145\ \text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$ for bilayer/trilayer devices (Fig. 1c). The high mobility of $> 100\ \text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$ uncovers the great potential of bilayer and trilayer MoS_2 for high-performance transistors. For 100-nm short-channel devices, the current density increases with the layer number, i.e. 0.40 (monolayer), 0.64 (bilayer) and 0.81 (trilayer) $\text{mA}/\mu\text{m}$. Remarkably, the short-channel trilayer device with 40-nm channel length exhibits a record-high on-current density of 1.70 $\text{mA}/\mu\text{m}$ at $V_{\text{ds}} = 2\ \text{V}$ and a high on/off ratio exceeding 10^7 . These device characteristics show high potential, with excellent electrostatic control and high drive current for end-of-roadmap transistors (Fig. 1d).

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Conflict of interest statement. None declared.

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