Single-Stage Wireless-Power-Transfer Resonant Converter with Boost Bridgeless Power-Factor-Correction Rectifier

Junwei Liu, Ka Wing Chan, *Member, IEEE,* C.Y. Chung, *Fellow, IEEE*, Nelson H. L. Chan, Ming Liu, and Wenzheng Xu

***Abstract*—Wireless power transfer (WPT) has drawn more and more attention and has many applications, such as wireless electric vehicle (EV) charging systems, that require high power, high efficiency and high power factor. In this paper, a single-stage WPT resonant converter with bridgeless boost power-factor-correction (PFC) rectifier is proposed to improve efficiency and power quality of line input, and reduce production cost and complexity for high power WPT system. The bridgeless single-stage topology is creatively proposed to apply in WPT system, which is much more advantageous than conventional two-stage WPT converter with individual boost PFC stage.**

***Index Terms*—wireless power transfer (WPT), bridgeless, single-stage, power factor correction (PFC)**

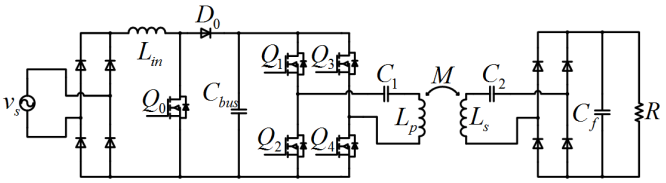

Fig. 1. Conventional AC/DC WPT resonant converter with boost PFC

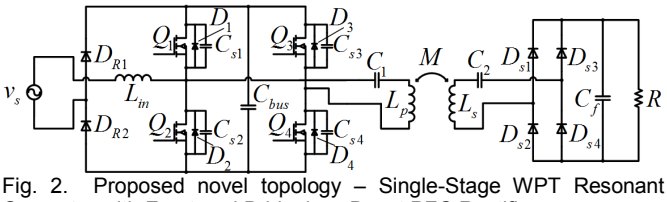

Fig. 2. Proposed novel topology – Single-Stage WPT Resonant Converter with Front-end Bridgeless Boost PFC Rectifier

I. Introduction

WIRELESS Power Transfer (WPT) is taking up more and more roles in industrial community. WPT technology has a variety of applications with power levels ranged from several milliwatts to tens of kilowatts, including charging portable telephone [1], supplying power for biomedical implants [2]-[4], electric vehicle (EV) battery charging [5], [6], and roadway powering moving EVs [7], [8]. Compared to conventional wired power transmission, WPT technology is much more advantageous: convenient, safe, and reliable. Inductive coupling method [1], [2], [6]-[14], as a traditional WPT technology, has been researched for a long time and is a very efficient way to deliver power wirelessly within a short distance. However, power and efficiency drop severely if transfer distance extends or there is a misalignment between transmitter and receiver. Another efficient WPT technology for mid-range transfer, magnetic resonant coupling approach [15]-[20], proposed and demonstrated by MIT in 2007 [21], attracts much interest from researchers in recent years, due to its high efficiency and relatively longer transfer distance. This approach utilizes resonance characteristic of coupled primary and secondary resonant tanks under a specific frequency to achieve WPT efficiently. A conventional WPT system consists of a single-phase electric power supply, a full-bridge rectifier, a boost power factor corrector (PFC), a dc bus capacitor, a high-frequency inverter, coupled primary and secondary resonant tanks, a secondary high-frequency rectifier-bridge, a filter capacitor and a load resistor, as shown in Fig. 1.

Traditional AC/DC converter with power factor correction usually employs a two-stage topology. The first stage is a boost PFC converter and the second is a DC/DC conversion stage. Like the WPT system in Fig. 1, the first stage includes a full-bridge rectifier and a boost PFC, and the second stage is a DC/DC WPT resonant converter. It is obvious that such two-stage topology cannot achieve the highest efficiency due to more power losses in the two-stage conversion while it is also not the most economical as more components would be required for two-stage conversion. In recent years, single-stage topologies [22], [23] that integrate both PFC and DC/DC conversion into one power conversion stage have been proposed to overcome the aforementioned drawbacks. Most existing researches are mainly focused on applying single-stage topologies in full -bridge converter [24], half-bridge converter [25], LLC converter [26]-[28], forward converter [29], flyback converter

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[30], [31], and so on, with most of them designed for small power applications. In this paper, a novel single-stage topology is proposed and applied to high power WPT systems with improved efficiency and lower cost. Furthermore, based on this single-stage technique, bridgeless boost PFC rectifiers [32]-[35] are introduced and integrated in the WPT system. Bridgeless boost PFC rectifiers would have less conduction loss due to less number of semiconductor devices being involved. Therefore, the newly proposed converter can reduce losses and cost further while the high performance of the PFC function can be maintained. Compared to the single-stage Z-source resonant converter proposed in [36] for WPT application, the newly proposed converter is advantageous in terms of efficiency and number of semiconductor devices and passive components.

In this paper, the topology description and analysis, power factor (PF) and total harmonics distortion (THD) analysis, modulation method and circuit operation of the proposed converter with a new control approach are first presented, and then, the design procedure with an example is proposed. In addition, a new and more accurate analytical and calculation method considering both the fundamental and higher-order components is also proposed to analyze the DC/DC WPT converter. Finally, an experimental prototype is implemented to verify the analysis and design.

II. Proposed Single-Stage Topology

A. Circuit Description

Fig. 2 shows the proposed novel topology – single-stage WPT resonant converter with bridgeless boost PFC rectifier, which ultimately integrates the front-end full-bridge rectifier, boost PFC, and full-bridge inverter in the primary side together. v_s is ac input voltage, D_{R1} and D_{R2} are front-end bridgeless rectifier diodes, L_{in} is input inductor, C_{bus} is bus capacitor, Q_1-Q_4 are four MOSFET switches (with body diodes D_1-D_4), C_{s1}-C_{s4} are snubber capacitors of the switches, C_1 and C_2 are capacitors of primary and secondary resonant tanks, L_p and L_s are inductors of primary and secondary resonant tanks, M is mutual inductance of L_p and L_s, D_{s1}-D_{s4} are secondary-side rectifier diodes, C_f is output filtering capacitor, and R is load resistor. Compared with the conventional topology in Fig. 1, a half bridge of the full-bridge rectifier, the switch Q_0, and the diode D_0 (totally four semiconductor devices) are eliminated. In the proposed topology, Q_1 and Q_2 perform two functions: (a) realization of PFC: they act as D_0 and Q_0 as shown in Fig. 1 for PFC, and (b) combination with Q_3 and Q_4 to form the full-bridge inverter of the DC/DC WPT resonant converter.

B. Bridgeless Boost Power-Factor-Correction rectifier

Fig. 3(a) shows the bridgeless boost PFC rectifier of the proposed topology, which consists of rectifier diodes D_{R1} and D_{R2}, input inductor L_{in}, half bridge switches Q_1 and Q_2, and bus capacitor C_{bus}. Fig. 3(b) shows the operations in positive and negative line cycle. In fact, whenever in positive or negative line cycle, the bridgeless boost PFC rectifier can act as a boost converter to fulfill PFC function. Here upper equivalent circuit in Fig. 3(b) is taken as an example to analyze its characteristics.

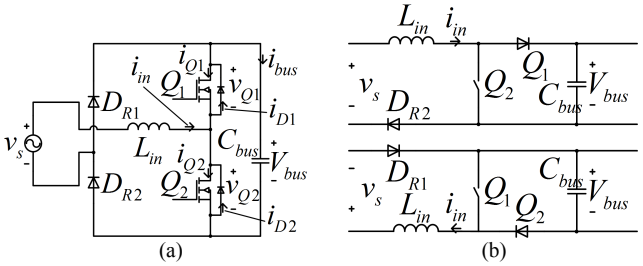


Fig. 3. Bridgeless boost PFC rectifier

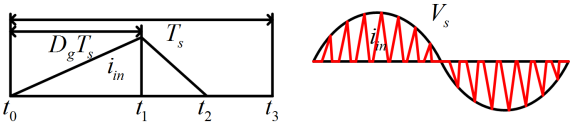


Fig. 4. Waveforms of input current

1) Working principle and analysis

As shown in Fig. 4, the input inductor must work in discontinuous conduction mode (DCM) in order to reduce the higher-order harmonics in the line current [25], [26], [30], and [37]. When switch Q_2 is on, voltage across L_{in} is v_s, and the input current i_{in} flowing through L_{in} is given by:

$$di_{in}/dt = v_s/L_{in}. \tag{1}$$

When Q_2 is off, v_{Q2} is equal to V_{bus} (bus voltage) and the voltage across L_{in} is v_s-V_{bus}, then i_{in} is given by:

$$di_{in}/dt = (v_s - V_{bus})/L_{in}. \tag{2}$$

For a complete cycle of switching period T_s, i_{in} is expressed as:

$$i_{in} = \begin{cases} (v_s/L_{in})\cdot t & t\in[t_0,t_1) \\ (V_{bus}/L_{in})\cdot(t_1-t_0)-((V_{bus}-v_s)/L_{in})\cdot t & t\in[t_1,t_2), \\ 0 & t\in[t_2,t_3] \end{cases} \tag{3}$$

where t_0-t_3 are defined as (D_g is duty ratio of the switch):

$$t_0 = 0, t_1 = D_g T_s, t_2 = D_g T_s\left(V_{bus}/(V_{bus}-v_s)\right), t_3 = T_s. \tag{4}$$

To make input inductor work in DCM, t_2 must be smaller than or equal to t_3, which means (peak value of v_s noted as V_{sp}):

$$D_g T_s\left(V_{bus}/(V_{bus}-v_s)\right) \le T_s \Rightarrow V_{sp}/V_{bus} \le 1-D_g. \tag{5}$$

Therefore, the average input power in a switching period T_s is:

$$P_T(t) = \left(\int_{t_0}^{t_3} v_s(t) i_{in} dt\right)/T_s = \frac{D_g^2 v_s(t)^2 T_s V_{bus}}{2L_{in}\left(V_{bus}-v_s(t)\right)}. \tag{6}$$

For a line cycle, the average input power is:

$$P_{in} = \left[\int_0^{T_l} P_T(t)dt\right]/T_l = \frac{D_g^2 V_{sp}^2}{2\pi L_{in} f_s}\int_0^{\pi}\frac{(\sin\alpha)^2}{1-m\sin\alpha}d\alpha, \tag{7}$$

where T_l is line period, and m is V_{sp}/V_{bus}.

2) Analysis of PF and THD$_i$

The average value of i_{in} during a switching period is given as:

$$i_{in.avg} = \frac{1}{T_s}\int_0^{T_s} i_{in}dt = D_g^2\cdot\frac{V_{sp}}{2L_{in}f_s}\cdot\frac{\sin(\omega_l t)}{1-m\left|\sin(\omega_l t)\right|}, \tag{8}$$

where ω_l is line frequency in radian. Because of the symmetric characteristics for both positive and negative half cycles of v_s, the root-mean-square (RMS) values of input current i_{in} for positive and negative half cycles of v_s are equal. Therefore, the RMS value of input current i_{in} for T_l is as follows:

$$i_{in.rms}=\frac{D_g{}^2V_{sp}}{2\sqrt{\pi}L_{in}f_s}\sqrt{\int_0^{\pi}\frac{(\sin\alpha)^2}{(1-m|\sin\alpha|)^2}d\alpha}. \quad (9)$$

Therefore, the PF of the proposed converter is obtained:

$$\mathrm{PF}=\left(\sqrt{2}\int_0^{\pi}\frac{(\sin\alpha)^2}{1-m\sin\alpha}d\alpha\right)\Bigg/\left(\sqrt{\pi}\sqrt{\int_0^{\pi}\frac{(\sin\alpha)^2}{(1-m\sin\alpha)^2}d\alpha}\right). \quad (10)$$

From (10), the PF of the proposed converter is only related to m (equal to V_{sp}/V_{bus}), as shown in Fig. 5 (curve in blue).

For $\mathrm{THD_i}$ (THD of input current i_{in}) analysis, $i_{in.avg}$ can be expressed as Fourier series:

$$\begin{aligned}&i_{in.avg}(t)=b_1\sin(\omega_l t)+b_3\sin(3\omega_l t)+b_5\sin(5\omega_l t)+\cdots,\\&b_n=(2/T_l)\int_0^{T_l}i_{in.avg}(t)\sin(n\omega_l t)dt\quad n=1,3,5,...,\end{aligned} \quad (11)$$

and $\mathrm{THD_i}$ can be obtained:

$$\mathrm{THD_i}=\sqrt{b_3{}^2+b_5{}^2+b_7{}^2+\cdots}/b_1. \quad (12)$$

By analysis and calculation, $\mathrm{THD_i}$ is also only related to m value, as shown in Fig. 5 (curve in green).

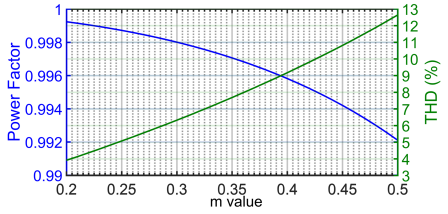


Fig. 5. Relations of m value vs PF and $\mathrm{THD_i}$

C. DC/DC WPT Resonant Converter

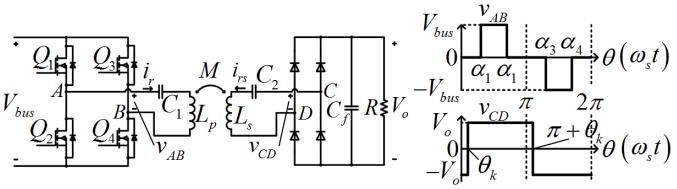


Fig. 6. DC/DC WPT resonant converter and waveforms of v_{AB} and v_{CD} for theoretical analysis.

After the front-end bridgeless boost PFC rectifier stage is the DC/DC WPT resonant converter applying resonant magnetic coupling technology to realize mid-range WPT. Such converter, also called DC/DC resonant converter for WPT, is shown as left part of Fig. 6, where V_{bus} is bus voltage, or DC input voltage of the converter, V_o is output voltage, v_{AB} and v_{CD} are voltages across primary and secondary sides of resonant tank. By adjusting switching sequence and duty ratios of switches Q_1-Q_4, v_{AB} can be regulated to be a three-level voltage with adjustable duty ratio D_{ab}, shown as right part of Fig. 6.

First Harmonic Approximation (FHA) [38], which only considers fundamental component, is commonly applied to analyze DC characteristics of resonant converters. If FHA is applied here, (13)-(15) will be obtained:

$$v_{AB}=\left[1/(j\omega_s C_1)+j\omega_s L_p\right]\cdot i_r+j\omega_s M\cdot i_{rs}, \quad (13)$$

$$0=j\omega_s M\cdot i_r+\left[1/(j\omega_s C_2)+j\omega_s L_s\right]\cdot i_{rs}+R_e\cdot i_{rs}, \quad (14)$$

$$v_{CD}=-i_{rs}\cdot R_e, \quad (15)$$

where R_e is equivalent resistor:

$$R_e=(8/\pi^2)\cdot R. \quad (16)$$

From (13)-(15), voltage transfer gain of the resonant tank can be obtained:

$$\left|\frac{v_{CD}}{v_{AB}}\right|=\sqrt{\left(L_p/M-1/(\omega_s{}^2C_1M)\right)^2+\left(\frac{\omega_s{}^4L_pL_sC_1C_2-\omega_s{}^2(C_2L_s+C_1L_p)+1}{\omega_s{}^3MC_1C_2R_e}-\frac{\omega_sM}{R_e}\right)^2}. \quad (17)$$

And DC voltage transfer gain is:

$$V_o/V_{bus}=\sin(D_{ab}\pi/2)\cdot|v_{CD}/v_{AB}|. \quad (18)$$

By analysis, there are three resonant frequencies [11]:

$$\begin{aligned}\omega_1&=\left[(L_p+M\cdot k)C_1\right]^{-1/2}=\left[(L_s+M/k)C_2\right]^{-1/2},\\\omega_2&=\left[(L_p-M\cdot k)C_1\right]^{-1/2}=\left[(L_s-M/k)C_2\right]^{-1/2},\\\omega_3&=(L_pC_1)^{-1/2}=(L_sC_2)^{-1/2},\end{aligned} \quad (19)$$

where k is defined as square root of L_p/L_s. Voltage transfer gain of the resonant tank is independent of load resistance at ω_1 and ω_2 while at ω_3, it is directly proportional to load resistance [39].

However, such approximation is not accurate enough for analyzing the converter when duty ratio and load power are small because there are non-negligible higher-order harmonics exiting in the circuit. For accurate analysis, both fundamental component and higher-order harmonics shall be considered.

Current flowing through L_s is always continuous at most load conditions except in very low load conditions. Therefore, in this paper only the conditions of L_s in continuous current mode are analyzed. By analyzing the behavior of the converter, v_{AB} is a three-level voltage with duty ratio D_{ab} and v_{CD} is a two-level voltage with 50% duty ratio, as shown in Fig. 6, where θ is equal to $\omega_s t$, ω_s is operating frequency in radian, θ_k is the phase angle of v_{CD}, and α_1-α_4 are defined as:

$$\alpha_{1,2}=(1\mp D_{ab})\pi/2,\alpha_{3,4}=(3\mp D_{ab})\pi/2. \quad (20)$$

Hence, v_{AB} and v_{CD} can be expressed as Fourier series:

$$v_{AB}=v_{AB.1}+v_{AB.3}+v_{AB.5}+\cdots+v_{AB.n}+\cdots, \quad (21)$$

$$v_{CD}=v_{CD.1}+v_{CD.3}+v_{CD.5}+\cdots+v_{CD.n}+\cdots, \quad (22)$$

where

$$v_{AB.n}=V_{AB.ns}\sin(n\omega_s t)+V_{AB.nc}\cos(n\omega_s t), \quad (23)$$

$$v_{CD.n}=V_{CD.ns}\sin(n\omega_s t)+V_{CD.nc}\cos(n\omega_s t), \quad (24)$$

and $V_{AB.ns}$, $V_{AB.nc}$, $V_{CD.ns}$, and $V_{CD.nc}$ (n=1, 3, 5 …) are calculated:

$$V_{AB.ns}=(-1)^{(n-1)/2}\cdot 4V_{bus}\sin(nD_{ab}\pi/2)/(n\pi),V_{AB.nc}=0, \quad (25)$$

$$V_{CD.ns}=4V_o\cos(n\theta_k)/(n\pi),V_{CD.nc}=-4V_o\sin(n\theta_k)/(n\pi). \quad (26)$$

i_r and i_{rs} are currents through L_p and L_s, v_{c1} and v_{c2} are voltages across C_1 and C_2, also shown in Fourier Series:

$$i_r=i_{r.1}+i_{r.3}+i_{r.5}+\cdots+i_{r.n}+\cdots, \quad (27)$$

$$i_{rs}=i_{rs.1}+i_{rs.3}+i_{rs.5}+\cdots+i_{rs.n}+\cdots, \quad (28)$$

$$v_{c1}=v_{c1.1}+v_{c1.3}+v_{c1.5}+\cdots+v_{c1.n}+\cdots, \quad (29)$$

$$v_{c2}=v_{c2.1}+v_{c2.3}+v_{c2.5}+\cdots+v_{c2.n}+\cdots, \quad (30)$$

where

$$i_{r.n}=I_{r.ns}\sin(n\omega_s t)+I_{r.nc}\cos(n\omega_s t), \quad (31)$$

$$i_{rs.n} = I_{rs.ns}\sin(n\omega_s t) + I_{rs.nc}\cos(n\omega_s t), \quad (32)$$

$$v_{c1.n} = V_{c1.ns}\sin(n\omega_s t) + V_{c1.nc}\cos(n\omega_s t), \quad (33)$$

$$v_{c2.n} = V_{c2.ns}\sin(n\omega_s t) + V_{c2.nc}\cos(n\omega_s t). \quad (34)$$

Applying Kirchhoff's Voltage Law, (35)-(38) are obtained:

$$v_{AB} = L_p(di_r/dt) + v_{c1} + M(di_{rs}/dt), \quad (35)$$

$$i_r = C_1(dv_{c1}/dt), \quad (36)$$

$$v_{CD} = L_s(di_{rs}/dt) + v_{c2} + M(di_r/dt), \quad (37)$$

$$i_{rs} = C_2(dv_{c2}/dt). \quad (38)$$

From (21)-(24), and (27)-(38), we have:

$$V_{AB.ns} = -Z_{pn}I_{r.nc} - Z_{mn}I_{rs.nc}, \quad (39)$$

$$V_{AB.nc} = Z_{pn}I_{r.ns} + Z_{mn}I_{rs.ns}, \quad (40)$$

$$V_{CD.ns} = -Z_{sn}I_{rs.nc} - Z_{mn}I_{r.nc}, \quad (41)$$

$$V_{CD.nc} = Z_{sn}I_{rs.ns} + Z_{mn}I_{r.ns}, \quad (42)$$

where Z_{pn}, Z_{mn}, and Z_{sn} (n=1, 3, 5 …) are defined as:

$$Z_{pn} = n\omega_s L_p - \frac{1}{n\omega_s C_1}, Z_{mn} = n\omega_s M, Z_{sn} = n\omega_s L_s - \frac{1}{n\omega_s C_2}. \quad (43)$$

Output power can be expressed as:

$$P_o = (1/\pi)\int_{\theta_k}^{\pi+\theta_k} V_o(-i_{rs})d\theta = V_o^2/R. \quad (44)$$

From characteristic of the secondary-side rectifier-bridge, at $\omega_s t=\theta_k$, i_{rs} is equal to zero, therefore,

$$i_{rs}(\theta_k) = i_{rs.1}(\theta_k) + i_{rs.3}(\theta_k) + \cdots + i_{rs.n}(\theta_k) + \cdots = 0. \quad (45)$$

And (46) and (47) can be derived from (20)-(45),

$$\frac{8V_oV_{bus}}{\pi^2}\sum_{n=1,3,5,\cdots}\frac{(-1)^{\frac{n-1}{2}}Z_{mn}\sin(nD_{ab}\pi/2)\sin(n\theta_k)}{n^2(Z_{pn}Z_{sn} - Z_{mn}^2)} = \frac{V_o^2}{R}, \quad (46)$$

$$\sum_{n=1,3,5,\cdots}\frac{(-1)^{\frac{n-1}{2}}Z_{mn}V_{bus}\sin(nD_{ab}\pi/2)\cos(n\theta_k) - Z_{pn}V_o}{n(Z_{pn}Z_{sn} - Z_{mn}^2)} = 0. \quad (47)$$

In this paper, balancing calculation complexity and accuracy, fundamental (1st-order), 3rd-order, and 5th-order components are considered in the calculation to analyze the DC characteristics of the proposed WPT resonant converter. By solving (46) and (47), V_o/V_{bus} and θ_k are calculated.

D. Modulation Method and Circuit Operation

1) Description of proposed modulation method

Usually frequency control methods are applied in variable kinds of resonant converters. However, frequency control method is not suitable for the proposed topology. From (7), (46) and (47), if D_{ab} is set constantly 1, by increasing operation frequency f_s, P_{in} and P_o will be regulated to low level. However, such regulation will lead to very large V_{bus}, usually larger than 1kV, which requires bus capacitor and all primary-side semiconductor devices with high voltage rating and causes severe EMI problem because of high dv/dt.

Here a new control approach is proposed to allow the proposed converter to work in a wide-range load condition with high performances (high efficiency, low THD, and high PF). In the proposed control method, D_{ab} is the control parameter to regulate output power with constant V_o when load varies, with f_s kept constant within the optimal range of the resonant tank. Make D_g=D_{ab}/2, then P_{in} is amended as:

$$P_{in} = (D_{ab}/2)^2\left(V_{sp}^2/(L_{in}\omega_s)\right)\int_0^{\pi}\left[(\sin\theta)^2/(1-m\sin\theta)\right]d\theta. \quad (48)$$

From (46)-(48), P_{in} and P_o can be easily regulated to low level by adjusting D_{ab} and will not cause very high bus voltage. Therefore, such control method is applied to give a wide-range load regulation.

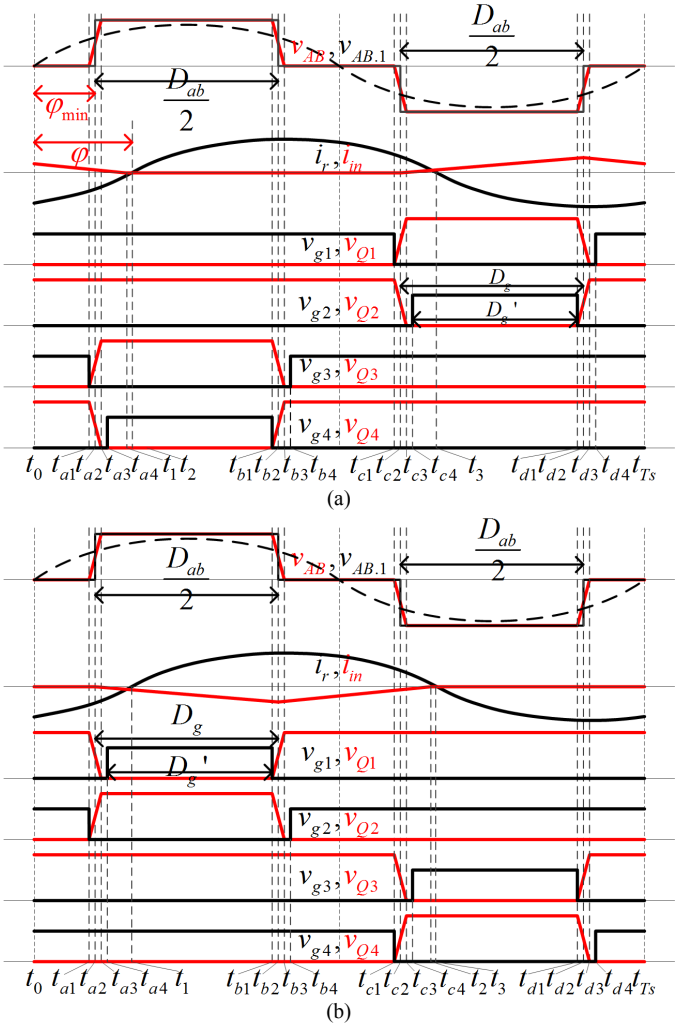


Fig. 7. Operation waveforms of the proposed modulation method: (a) when v_s is in its positive cycle; (b) when v_s is in its negative cycle.

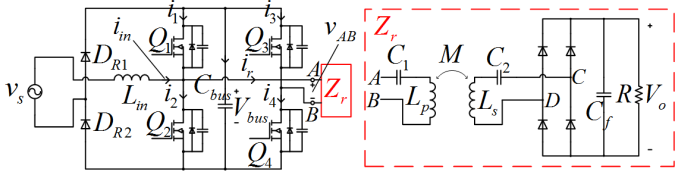


Fig. 8. Equivalent circuit of the proposed topology with resonant tank and secondary side equivalent to impedance Z_r

2) Modulation and Operation Analysis

The proposed modulation and operation waveforms are shown in Fig. 7. Duty ratios of v_{g1} and v_{g2} are noted as D_{g1} and D_{g2}, respectively. Duty ratios of v_{g1} and v_{g2} are complimentary, so are those of v_{g3} and v_{g4}. When v_s is in its positive cycle, D_{g2} is equal to D_g' and v_{g4} leads v_{g2} half a switching period; when v_s is

in its negative cycle, D_{g1} is equal to D_g' and v_{g3} lags v_{g1} half a switching period. In an ideal condition, D_g' is equal to D_g. However, in practical implementation considering dead time, D_g' is smaller than D_g. Such modulation method generates a three-level voltage with an adjustable duty ratio. For operation analysis, the proposed topology is simplified to an equivalent circuit shown in Fig. 8.

Stage 1 (t_0-t_{a1}): From t_0 to t_{a1}, Q_1 and Q_3 are on while Q_2 and Q_4 are off. Current flows through v_s, L_{in}, Q_1, C_{bus}, D_{R2}, Q_3, and Z_r, as shown in Fig. 9(a).

Stage 2 (t_{a1}-t_{a4}): At t_{a1}, Q_3 is turned off; C_{s3} starts to be charged and C_{s4} starts to be discharged. From t_{a1} to t_{a3}, current flows through v_s, L_{in}, Q_1, C_{bus}, D_{R2}, C_{s3}, C_{s4}, and Z_r, as shown in Fig. 9(b). At t_{a3}, C_{s3} is charged to V_{bus} and C_{s4} is discharged to zero. From t_{a3} to t_{a4}, current flows through v_s, L_{in}, Q_1, C_{bus}, D_{R2}, D_4, and Z_r, as shown in Fig. 9(c).

Stage 3 (t_{a4}-t_{b1}): At t_{a4}, Q_4 is turned on. From t_{a4} to t_{b1}, Q_1 and Q_4 are on while Q_2 and Q_3 are off. At t_1, input current i_{in} reaches zero. From t_{a4} to t_1, current flows through v_s, L_{in}, Q_1, C_{bus}, D_{R2}, Q_4, and Z_r, as shown in Fig. 9(d). At t_2, i_r changes polarity from negative to positive. From t_1 to t_{b1}, current flows through Q_1, C_{bus}, Q_4, and Z_r, as shown in Fig. 9(e)(f).

Stage 4 (t_{b1}-t_{b4}): At t_{b1}, Q_4 is turned off; C_{s3} and C_{s4} start to be discharged and charged respectively. From t_{b1} to t_{b3}, current flows through Q_1, Z_r, C_{s3}, C_{s4}, and C_{bus}, as shown in Fig. 9(g). At t_{b3}, voltages of C_{s3} and C_{s4} reach zero and V_{bus}. From t_{b3} to t_{b4}, current flows through Q_1, Z_r, and D_3, as shown in Fig. 9(h).

Stage 5 (t_{b4}-t_{c1}): At t_{b4}, Q_3 is turned on. From t_{b4} to t_{c1}, Q_1 and Q_3 are on while Q_2 and Q_4 are off. Current flows through Q_1, Z_r, and Q_3, as shown in Fig. 9(i).

Stage 6 (t_{c1}-t_{c4}): At t_{c1}, Q_1 is turned off; C_{s1} and C_{s2} start to be charged and discharged respectively. From t_{c1} to t_{c3}, current flows through C_{s1}, C_{s2}, Z_r, Q_3, and C_{bus}, as shown in Fig. 9(j). At t_{c2}, i_{in} starts to increase from zero. From t_{c2} to t_{c3}, current flows through v_s, L_{in}, C_{s1}, C_{s2}, Z_r, Q_3, C_{bus}, and D_{R2}, as shown in Fig. 9(k). At t_{c3}, C_{s1} is charged to V_{bus} and C_{s2} is discharged to zero. From t_{c3} to t_{c4}, current flows through v_s, L_{in}, D_2, Z_r, Q_3, C_{bus}, and D_{R2}, as shown in Fig. 9(l).

Stage 7 (t_{c4}-t_{d1}): At t_{c4}, Q_2 is turned on. From t_{c4} to t_{d1}, Q_2 and Q_3 are on while Q_1 and Q_4 are off. Current flows through v_s, L_{in}, Q_2, Z_r, Q_3, C_{bus}, and D_{R2}, as shown in Fig. 9(m)(n). At t_3, i_r changes polarity from positive to negative.

Stage 8 (t_{d1}-t_{d4}): At t_{d1}, Q_2 is turned off; C_{s1} starts to be discharged and C_{s2} starts to be charged. From t_{d1} to t_{d3}, current flows through v_s, L_{in}, C_{s1}, C_{s2}, C_{bus}, Q_3, Z_r, and D_{R2}, as shown in Fig. 9(o). At t_{d3}, C_{s1} is discharged to zero and C_{s2} is charged to V_{bus}. From t_{d3} to t_{d4}, current flows through v_s, L_{in}, D_1, V_{bus}, D_{R2}, Q_3, and Z_r, as shown in Fig. 9(p).

Stage 9 (t_{d4}-t_{Ts}): At t_{d4}, Q_1 is turned on, and this stage is the same with Stage 1, as shown in Fig. 9(q).

3) Operation frequency selection

In order to realize soft-switching of all the four switches in the proposed converter with the proposed modulation method, operation frequency f_s should be selected properly. Firstly, By analyzing the operation of the converter, i_1-i_4 as defined and shown in Fig. 8 have to be positive at the instances of Q_1-Q_4 turning-off, respectively, so as to achieve soft-switching in all

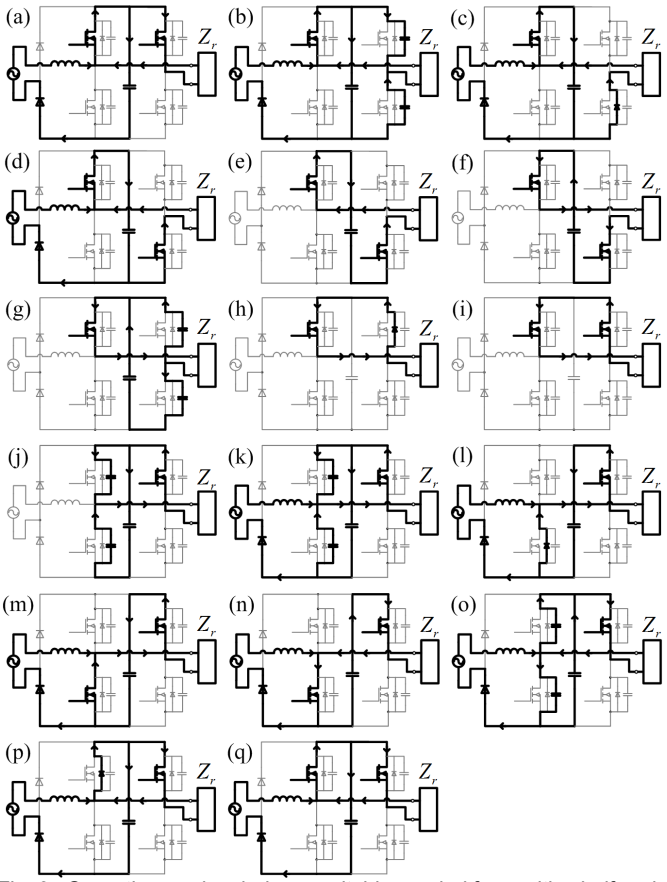


Fig. 9. Operation modes during a switching period for positive half cycle of input line voltage v_s.

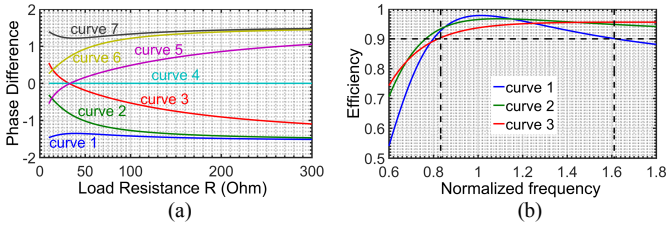


Fig. 10. (a) Phase difference vs R at different operation frequencies; (b) Efficiency vs normalized frequency at different load conditions.

four switches. Therefore, phase difference of $v_{AB.1}$ and i_r (defined as φ) must satisfy the following:

$$\varphi > \left[\left(1-D_{ab}\right)/2\right]\pi. \tag{49}$$

From (13)-(15), φ only varies with equivalent load resistance R_e (if operation frequency f_s is confirmed):

$$\varphi = \angle\frac{v_{AB}}{i_r} = \angle\left(j\omega_s L_p - \frac{j}{\omega_s C_1} + \frac{\omega_s^2 M^2}{j\omega_s L_s - j/\left(\omega_s C_2\right) + R_e}\right). \tag{50}$$

Fig. 10(a) shows the curves of phase difference vs load resistance at different operation frequencies (curve 1: $\omega_s<\omega_1$; curve 2: $\omega_s=\omega_1$; curve 3: $\omega_1<\omega_s<\omega_3$; curve 4: $\omega_s=\omega_3$; curve 5: $\omega_3<\omega_s<\omega_2$; curve 6: $\omega_s=\omega_2$; curve 7: $\omega_s>\omega_2$). To obtain enough large φ, curve 6 and 7 should be selected. However, from (46) and (47), P_o will be infinitely large if ω_s is equal to ω_2. Therefore, ω_s should be larger than ω_2. Considering total equivalent series resistance (ESR) of the resonant tank, transmission efficiency characteristics of the resonant tank can be obtained at base frequency ω_3, assuming ESR of primary

and secondary sides to be 0.3Ω, as shown in Fig. 10(b) (curve 1: R=40Ω; curve 2: R=100Ω; curve 3: R=200Ω). To maintain high efficiency, ω_s is suggested to be smaller than $1.6\omega_3$.

III. Design Procedure and Considerations

A. Design Procedure

To facilitate production design of the proposed converter, a 2.56kW laboratory prototype was designed to verify the proposed idea. The design procedures are described as follows:

1) Requirements of input and output

The input line voltage v_s is designed to be $220V_{rms}$, 50Hz. Maximum output power $P_{o.max}$ is 2.56kW, with constant output voltage V_o=320V. Thus, maximum output current $I_{o.max}$ is 8A.

2) Requirements and design of resonant coils

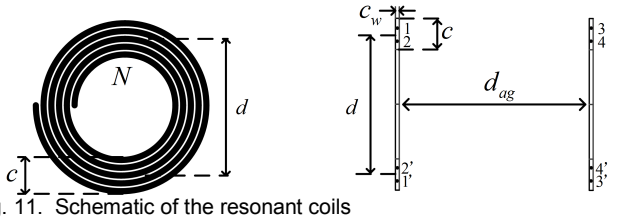


Fig. 11. Schematic of the resonant coils

Firstly, the parameters of resonant coils need to be fixed. To simplify the design and calculations, the two coils (air-core) are designed to be identical in spiral shape with the same wire type, mean coil diameter d, winding thickness c, and coils number N, as shown in Fig. 11. The operation frequency is set around 110kHz in order to comply with the industrial wireless charging standard (SAE J1773). Skin effect is considered and then skin depth d_{sk} is obtained as:

$$d_{sk} = \sqrt{\left(\rho/\left(\pi f_s \mu\right)\right)} \approx 0.2mm, \tag{51}$$

where ρ and μ are resistivity and permeability of copper. Therefore, copper litz wire is used to reduce the skin effect. The diameter of each thin wire strand should be smaller than twice of d_{sk}, 0.4mm. Hence, the litz wire with the following parameters was chosen: diameter of each strand d_{st} is 0.2mm; number of strands is 100; effective cross section area of the wire s_w is 3.14mm^2; diameter of the wire c_w is 3.0mm.

From [40], self-inductances of primary and secondary coils can be expressed as:

$$L_p = L_s = \frac{0.3937\left(\left(d/2\right)\times 100\right)^2 \cdot N^2 \cdot 10^{-6}}{8\left(\left(d/2\right)\times 100\right)+11\left(c\times 100\right)} = k_L N^2. \tag{52}$$

In practical implementation, c is determined by c_w, N, and air gap of loops c_{ag} (usually c_{ag} is 1.0mm):

$$c = N\left(c_w + c_{ag}\right). \tag{53}$$

For mutual inductance calculation, primary coil is represented by two equivalent filaments 1, 1' and 2, 2', and secondary coil by 3, 3' and 4, 4', as shown in Fig. 11. Mutual inductance of the two coils can be calculated by:

$$M = N^2 M_0, \tag{54}$$

$$M_0 = \left(M_{13}+M_{14}+M_{23}+M_{24}\right)/4, \tag{55}$$

$$M_{ij} = f_k\left(r_i, r_j, d_{ag}\right)\cdot\sqrt{r_i \cdot r_j}\times 10^{-4}, \tag{56}$$

where f_k is the function of k'^2, obtained from tables in [41] and:

$$k'^2 = \left[\left(r_i - r_j\right)^2 + {d_{ag}}^2\right]\Big/\left[\left(r_i + r_j\right)^2 + {d_{ag}}^2\right], \tag{57}$$

where d_{ag} is air gap distance of two coils and

$$r_1 = r_3 = \left(d/2\right)\left[1 + {c_w}^2/\left(6d^2\right)\right] + \sqrt{\left(c^2 - {c_w}^2\right)/12}, \tag{58}$$

$$r_2 = r_4 = \left(d/2\right)\left[1 + {c_w}^2/\left(6d^2\right)\right] - \sqrt{\left(c^2 - {c_w}^2\right)/12}. \tag{59}$$

For the application of wireless EV charging with typical automobile chassis size and height, d and d_{ag} are designed to be 500mm and 200mm, respectively. Considering in a loosely coupled WPT system the coupling coefficient of two coils is around 0.1-0.3 [11], [42], the coupling coefficient k_{ps} is assumed to be 0.18, which also satisfies

$$k_{ps} = M\Big/\sqrt{L_p L_s} = M_0/k_L. \tag{60}$$

With above known parameters and from (52)-(60), N is calculated to be 16. L_p and L_s are calculated to be 249.2μH and M is 44.8μH. In practical implementation, the measured values of L_p, L_s, and M are 241μH, 241μH, and 46μH, respectively.

Because of high core loss and low power density of coils with magnetic cores operating at high frequency (>100kHz), the resonant coils are designed without magnetic cores [9], [11]. In practical applications, shielding should be designed for WPT system, however in the laboratory environment without strict EMI requirements, shielding is not designed for the prototype. There are existing researches on shielding design for WPT system [43]-[45], among which [44] using resonant reactive shielding coil is suitable for air-core coils.

3) Resonant capacitors and operation frequency

The operation frequency f_s is chosen to be around 110kHz. Make the higher resonant frequency [11] f_2 equal to 110kHz and resonant capacitors are obtained by (19), which are measured to be 11.83nF in practical implementation. Then the accurate higher resonant frequency is revised to be 104.8kHz. Applying the proposed modulation method, D_{ab} is used to regulate the output voltage as load varies to maintain constant output voltage. When D_{ab} is equal to 1, output power should reach maximum 2.56kW. In such condition, with the known parameters (L_p, L_s, M, C_1, C_2, V_{sp}, and V_o), assuming f_s to be 106kHz (a little higher than 104.8kHz), from (46)-(48), m is calculated to be 0.87 which cannot satisfy (5). Therefore, f_s needs to be revised. By calculation, f_s is chosen to be 111.6kHz, at which m is equal to 0.49 satisfying (5).

4) Input inductance L_{in}

From above, when in maximum output condition, operation parameters are obtained: D_{ab}=1; P_{in}=2.56kW; f_s=111.6kHz; m=0.49. Therefore, from (48), L_{in} is calculated to be 36.9μH. In practical implementation, L_{in} is measured to be 37.0μH. Here, L_{in} is designed to be air-core inductor because of high core loss and low power density if using a magnetic-core inductor. In the experimental prototype, appropriate measures are implemented to avoid the EMI problem due to the air-core inductor.

5) Load range and maximum bus voltage

Ideally P_{in} is equal to P_o and then (44) and (46)-(48) form a non-linear equation set with three unknown parameters m, D_{ab}, and θ_k. By solving the equation set, V_{bus} and D_{ab} at different load conditions are calculated, as shown in Table I. By calculations and analysis, at low load conditions, m value decreases with load power decreasing. Therefore, the minimum

TABLE I
OPERATION POINTS AT DIFFERENT LOAD CONDITIONS

Load Condition	P_o (W)	V_{bus} (V)	D_{ab}
100%	2560	637	1
80%	2048	600	0.88
60%	1536	592	0.75
40%	1024	622	0.63
20%	512	745	0.47

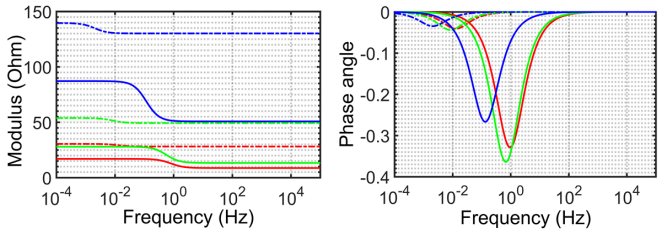


Fig. 12. Input impedance characteristics of the proposed converter at different load condition: Red curves: 100% load; Green curves: 60% load; Blue curves: 20% load and solid lines are those with instant line voltage 311V; dotted lines are those with instant line voltage 50V.

output power is limited by minimum m value (maximum V_{bus}). Here the minimum output power is set as 20% of rated output power, which is 512W, and the corresponding m value is 0.417. Therefore, maximum bus voltage is 745V.

6) Design of input EMI filter

To design the input EMI filter of the proposed converter, the input impedance of the proposed converter needs to be obtained. Because input part of the proposed converter acts as a DCM boost PFC converter, input impedance characteristics can be analyzed like that of a DCM boost PFC converter. From [46], input impedance of the proposed converter Z_{ic} is given as:

$$Z_{ic}=\frac{8L_{in}f_s\left(V_{bus}-v_s\right)}{{D_{ab}}^2V_{bus}}\frac{1+s\Big/\left(\dfrac{{D_{ab}}^2}{8L_{in}C_{bus}f_s}\dfrac{{v_s}^2\left(2V_{bus}-v_s\right)}{{V_{bus}}^2\left(V_{bus}-v_s\right)}\right)}{1+s\Big/\left(\dfrac{{D_{ab}}^2}{8L_{in}C_{bus}f_s}\dfrac{{v_s}^2\left(2V_{bus}-v_s\right)}{{V_{bus}}^2\left(V_{bus}-v_s\right)}\right)}. \quad (61)$$

From Fig. 12, at line frequency 50Hz, input impedance of the proposed converter is almost resistive at all load conditions, which can be noted as the input resistance R_{in}. Minimum R_{in} occurs in 100% load condition with v_s to be V_{sp} (311V) and maximum R_{in} occurs in 20% load condition with v_s to be zero:

$$\begin{aligned}R_{in.\min}&\approx\left(8L_{in}f_s\Big/{D_{ab.100\%}}^2\right)\left(1-V_{sp}\Big/V_{bus.100\%}\right)^2=8.7\Omega,\\ R_{in.\max}&\approx 8L_{in}f_s\Big/{D_{ab.20\%}}^2=149.5\Omega.\end{aligned} \quad (62)$$

A LC low-pass filter is implemented with inductor and capacitor noted as L_{if} and C_{if}. Assuming voltage out from input EMI filter is ideally the same as input voltage, in order to avoid phase-shift of input current, impedance of C_{if} at 50Hz is required to be much larger than $R_{in.max}$:

$$1\Big/\left(\omega_l C_{if}\right)\gg R_{in.\max}\Rightarrow C_{if}\ll 21.3\mu F. \quad (63)$$

Therefore, C_{if} is designed to be 1.0μF. And, in order to make voltage out from input EMI filter close to input voltage as much as possible, impedance of L_{if} at 50Hz is required to be much smaller than $R_{in.min}$:

$$\omega_l L_{if}\ll R_{in.\min}\Rightarrow L_{if}\ll 27.5mH. \quad (64)$$

Hence, L_{if} is designed to be 1.0mH with measured equivalent series resistance (ESR) R_{lf} to be 0.1Ω. With the parameters, output impedance of the input EMI filter is:

$$Z_{of}=\frac{\left(1\Big/\left(sC_{if}\right)\right)\left(sL_{if}+R_{lf}\right)}{1\Big/\left(sC_{if}\right)+sL_{if}+R_{lf}}=\frac{sL_{if}+R_{lf}}{s^2L_{if}C_{if}+sR_{lf}C_{if}+1}. \quad (65)$$

And therefore transfer function of the input EMI filter is:

$$F_f=Z_{ic}\Big/\left[Z_{ic}+Z_{of}\right]=1\Big/\left[1+Z_{of}\Big/Z_{ic}\right]. \quad (66)$$

By calculation and analysis, Z_{of}/Z_{ic}, regarded as the open loop gain, fulfilled the Nyquist stability criterion at different load conditions. Hence, there is no possible instability problem due to interaction with the input EMI filter.

Because current flowing through L_{if} is 50Hz, core loss is very small and can be ignored compared to copper loss. Hence, the loss of the input EMI filter can be calculated by:

$$P_{f.loss}={i_{in.rms}}^2\cdot R_{lf}, \quad (67)$$

where $i_{in.rms}$ can be calculated with (9). Therefore, at 100% load condition, loss of input EMI filter is calculated to be 13.6W, about 0.5% of the load power, which is acceptable.

B. Design summary and laboratory prototype

TABLE II
PARAMETERS OF THE LABORATORY PROTOTYPE

Components	Details
L_{in}	37.0μH (air core inductor)
D_{R1}, D_{R2}	IXYS DSEI 2x31-10B
Q_1, Q_2, Q_3, Q_4	CREE CAS120M12BM2
C_{bus}	4950μH, 900V (electrolytic capacitors bank)
C_{s1}, C_{s2}	5nF, 1kV (polypropylene capacitors)
C_{s3}, C_{s4}	1nF, 1kV (polypropylene capacitors)
L_p, L_s, M	241μH; 241μH; 46μH
C_1, C_2	11.83nF; 11.83nF (5kV polypropylene capacitors)
D_{s1}, D_{s2}, D_{s3}, D_{s4}	Vishay VS-30EPH06PbF
C_f	220μF, 450V (electrolytic capacitor)
L_{if}, C_{if}	1.0mH, 1.0μF

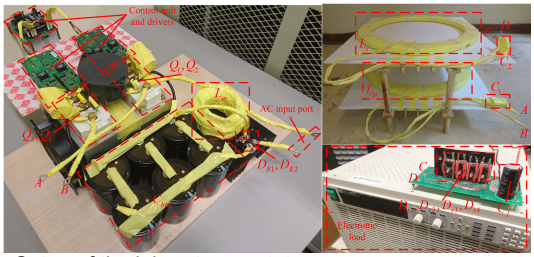


Fig. 13. Setup of the laboratory prototype

Table II shows the design summary and component selection of the laboratory prototype. For Q_1-Q_4, 2 SiC half-bridge Mosfet modules with 1.2kV voltage rating are used. Fig. 13 shows the setup of the laboratory prototype.

IV. EXPERIMENTAL RESULTS

Referring to the proposed design procedure, the laboratory prototype with rated (100% load) 2.56kW output is built and tested at different load conditions. Fig. 14 shows the waveforms of AC line input voltage and current and Fig. 20(b) shows the PF of AC line input and THD of AC line current (THD_i). At rated load condition, the PF and THD_i reach 0.99 and 15.4%, respectively. Overall, from 20% to 100% load range, the PF is over 0.97 and THD_i is below 22%. The AC line input voltage is not completely a pure sinewave (with measured THD 3%). If AC line input voltage's THD is close to zero, then THD_i can be 3%-4% further lower than present measured values. Fig. 20(a)

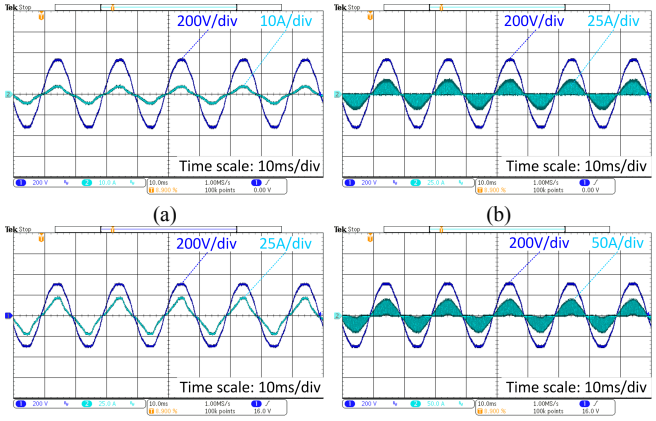


Fig. 14. Input voltage (in dark blue) and current (in light blue): (a) with EMI filter, 20% load; (b) without EMI filter, 20% load; (c) with EMI filter, 100% load; (d) without EMI filter, 100% load.

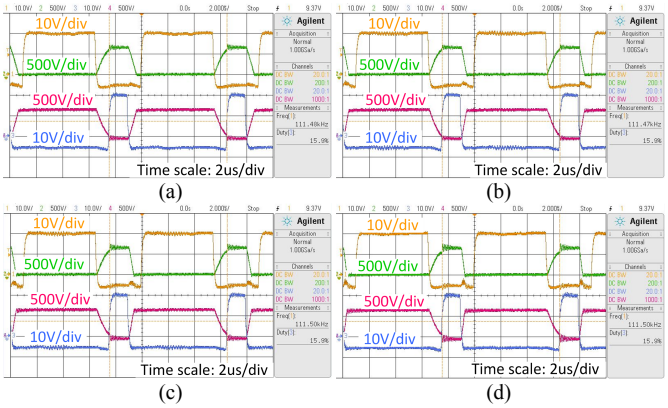


Fig. 15. Switching waveforms of Q_1 and Q_2 with 20% load under different phase of input line voltage: (a) 0; (b) π/6; (c) π/3; (d) π/2. (v_{g1} and v_{Q1} in yellow and green; v_{g2} and v_{Q2} in blue and violet)

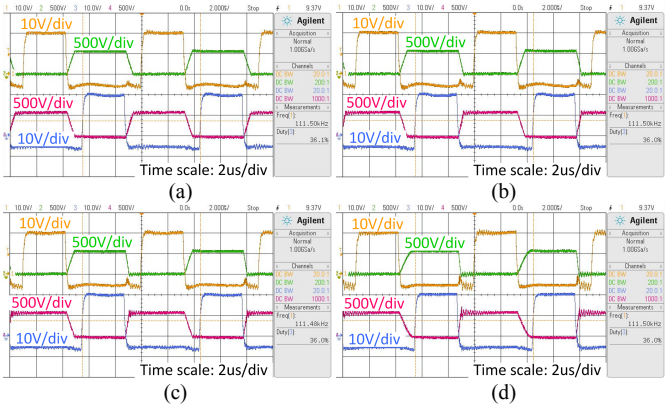


Fig. 16. Soft switching waveforms of Q_1 and Q_2 with 100% load under different phase of input line voltage: (a) 0; (b) π/6; (c) π/3; (d) π/2. (v_{g1} and v_{Q1} in yellow and green; v_{g2} and v_{Q2} in blue and violet)

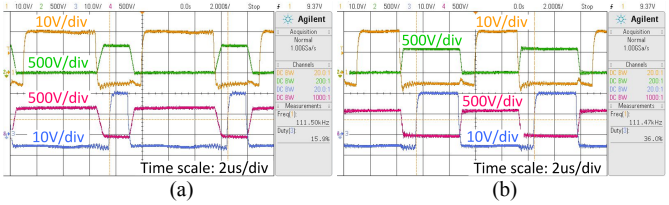


Fig. 17. Soft switching waveforms of Q_3 and Q_4: (a) 20% load; (b) 100% load. (v_{g3} and v_{Q3} in yellow and green; v_{g4} and v_{Q4} in blue and violet)

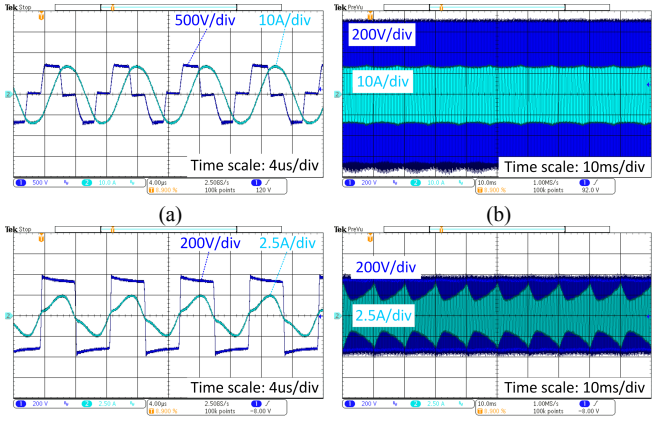


Fig. 18. Voltage (in dark blue) and current (in light blue) of resonant tank under 20% load condition: (a) primary side, high frequency profile; (b) primary side, low frequency (50Hz) profile; (c) secondary side, high frequency profile; (d) secondary side, low frequency (50Hz) profile.

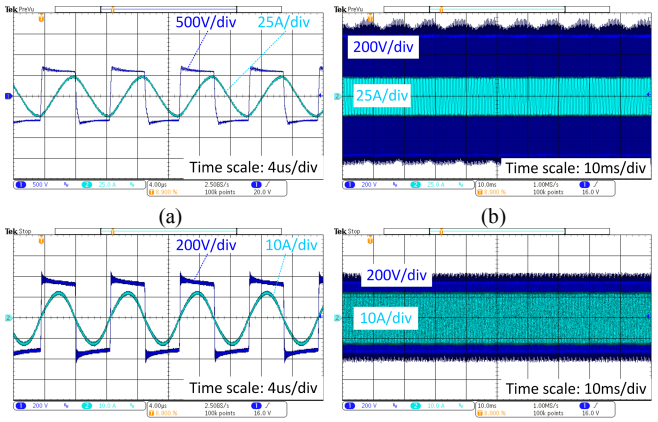
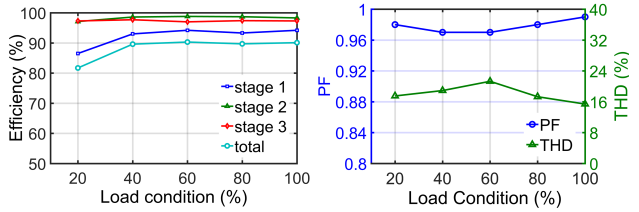


Fig. 19. Voltage (in dark blue) and current (in light blue) of resonant tank under 100% load condition: (a) primary side, high frequency profile; (b) primary side, low frequency (50Hz) profile; (c) secondary side, high frequency profile; (d) secondary side, low frequency (50Hz) profile.

shows the total efficiency and partial efficiencies at different stages (Stage 1: from AC line input to input port (AB) of resonant tank; stage 2: from input port (AB) to output port (CD) of resonant tank; stage 3: from output port (CD) of resonant tank to load). At rated load condition, total efficiency reaches 90.1% and efficiency of resonant tank (stage 2) reaches 98.3%. From 40% to 100% load range, total efficiency maintains as high as 90%. However, at 20% load condition, total efficiency drops to 81.7% because switching loss of Q_1 and Q_2 increases as soft-switching cannot be realized completely due to insufficient resonant current. Fig. 15 shows the switching waveforms of Q_1 and Q_2 at 20% load condition. Fig. 16 shows the soft-switching waveforms of Q_1 and Q_2 at 100% load condition. Fig. 17 shows the soft-switching waveforms of Q_3 and Q_4 at both 20% and 100% load conditions. Fig. 18 and Fig. 19 show the voltage and current waveforms of resonant tank at 20% and 100% load condition respectively. For comparison, a traditional two-stage topology for WPT with separate boost DCM PFC and a traditional topology for WPT without PFC are built up and tested. Table III shows the comparisons results at 100% load condition in terms of efficiency, PF, THD_i, and number of semiconductor devices. The Z-source resonant converter with PFC for WPT proposed in [36] is also compared

TABLE III
COMPARISON OF WPT SYSTEM TOPOLOGIES

Topologies	Efficiency (%)	Power Factor	THD_i (%)	Number of Semiconductor devices
Proposed single-stage WPT converter	90.1	0.99	15.4	6 diodes + 4 switches
Traditional two-stage converter for WPT	86.8	0.99	15.7	9 diodes + 5 switches
Traditional converter without PFC for WPT	92.2	0.69	96.5	8 diodes + 4 switches
Z-source converter with PFC for WPT	72.1	0.987	15.67	8 diodes + 4 switches



(a) (b)

Fig. 20. (a) Efficiencies under different load conditions at different stages; (b) PF and THD_i under different load conditions.

in Table III. Generally, the proposed topology exhibits its advantages compared to the other three topologies.

V. CONCLUSION AND FUTURE WORK

In this paper, a single-stage topology with bridgeless boost PFC rectifier is proposed to apply in high power WPT system, for the first time. Compared to traditional WPT system with a separate boost PFC converter, the proposed topology is more efficient and economical because of less number of semiconductor components. Detailed analysis of the proposed topology, design procedure and example are presented. Finally, a 2.56kW experimental prototype is implemented and tested to prove its high efficiency, PFC functionality, and economy. Future research will focus on improving its efficiency and reducing bus voltage of the proposed topology at light load conditions as well as issues in EMI and shielding.

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