Cascaded Voltage Control for Electric Springs with DC-Link Film Capacitors

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***Abstract*—For the conventional configuration of the single-phase electric springs, the electrolytic capacitor (E-cap) is required for buffering the double-line-frequency DC-link power. This demands large capacitance and constant average DC-link voltage for achieving sufficiently low voltage ripples of the E-cap, which renders low efficiency and poor reliability of the ES. To address these issues, a cascaded voltage control scheme is proposed in this paper. The proposed control scheme enables large fluctuations of the DC-link voltage so that the film capacitor (F-cap), which is of smaller capacitance and higher reliability, can be applied. Besides, the proposed control scheme can adaptively adjust the average DC-link voltage for achieving the minimum power loss of the ES. The quasi-steady-state and steady-state models of the electric-spring-based smart load are developed. The optimum average DC-link voltage for achieving the minimum power loss is analytically derived. The functionality and loss reduction capability of the proposed controller are verified through hardware experiments and simulations.**

***Index Terms*—AC microgrid, Electric springs, Reactive power control, Voltage control.**

I. Introduction

Microgrids, which are the clusters of low-voltage peripheral appliances, have been generally considered as flexible platforms for hosting the renewable generation (RG) without degrading the power quality and stability of the utility grids [1]. However, the volatility and intermittency of the integrated RG will render voltage fluctuations at the points of common coupling (PCC). This hinders the normal operation of the critical loads (CLs) in microgrids [2]. To address this issue, sufficient spinning reserves and energy storage systems are conventionally deployed for buffering the power imbalance between generation and demands [3]. Ironically, this will lead to the inefficient idle operations of generators and incur extra infrastructural investments, which is against the original intention of integrating RG [4].

The state-of-the-art technologies for voltage regulation can be classified as (i) generation side management (GSM) [5]–[7] and (ii) demand side management (DSM) [8]–[10]. For GSM methods, the grid-interfaced converters of RG are operated away from the maximum power point (MPP) and provide reactive power support for microgrids, which curtails the harvested renewable energy and extends the payback period [6]. Considering the heterogenous power quality requirements of different loads in microgrids [11], the DSM technologies offer a more cost-effective way of engaging the non-critical loads (NCL) in power balancing [12]. The intermittent part of the renewable energy can be buffered as heat in electrically-heated buildings, cold storage of refrigerators [13] and pulp in the paper industry [14], while the stable voltage supply can be provided for the CLs. From the perspective of implementation mechanism, the reported DSM technologies can be further categorized as (i) discrete DSM [8], which performs the on-off control of loads, and (ii) continuous DSM [10], which generally requires the switch-mode power converters to conduct the smooth load adjustments. By comparison, the continuous DSM can achieve a more elastic load control with insignificant increase of cost, which makes it feasible for taming the intermittency of RG in microgrids.

The single-phase electric springs (ES) have been proposed as a distributed and continuous DSM technology [15]. They are connected in series with different types of NCLs to form smart loads. The power profiles of these smart loads will be adaptively manipulated for compensating the power variations in power system [16]. It distinguishes itself from other DSM technologies with the advantages of (i) on-site voltage support [17], (ii) partial power processing [18] and (iii) automatic load tracking generation [19]. These features contribute to the significant reduction of required storage capacity in microgrids [20]. It is reported in [21] that the PV panels can be integrated with the ES for balancing the supplies and demands. A generalized phase angle control scheme is proposed in [22] to achieve the active and reactive power compensation by using the ES-based smart load. In [23], multiple ES are deployed in AC microgrids to enable a transactive energy system with automatic DSM function. To coordinate the operation of distributed ES, the consensus control scheme is proposed in [24]. To further reduce the required storage capacity of multiple ES and avoid the use of communication system [25], a decentralized control scheme is proposed in [26]. In [19], the conventional input-voltage control scheme is proposed for ES to achieve the reactive power control. This method does not consider the model of the NCL and cannot achieve a sufficiently fast transient response. A δ control method is proposed in [27] to determine the steady-state operating point of ES. However, this control method is impractical due to the need of detailed grid parameters. In [28], a simplified dynamic modular model of smart load is proposed for system-level control and management. Though the order of the model is reduced and predominant dynamics

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of the smart load are preserved, this model is based on basic proportional-integral (PI) control strategy. A radial-chordal decomposition (RCD) control method is reported in [29] for ES to achieve the decoupled control of power factor and PCC voltage. In the reported research work, the E-cap is generally required to store the double-line-frequency DC-link power and the average voltage of the E-cap is regulated to a constant value irrespective of the steady-state operating conditions of ES. This results in unnecessary and consistently-high voltage stress on the passive circuit components [30], which induces the unnecessary power loss and degrades the reliability of ES [31].

In order to improve the reliability of circuits and reduce the use of E-caps, the power decoupling technology has been reported to actively buffer the pulsating power in single-phase converters. With the addition of extra reactive storage components and active switches, the charging and discharging phases of storage components can be incorporated in the switching phases of the single-phase converters. Typical circuit topologies include (i) dedicated series and shunt DC active power filters, such as buck [32], boost [33], full-bridge [34] and series-stacked [35] topologies and (ii) integrated design of power-decoupled inverters, such as the DC split capacitors [36], interlinking capacitors between DC and AC terminals [37], flying capacitors [38] and integrated current choppers [39]. Although the power decoupling technology can effectively enhance the reliability of the inverters, the additional circuit components will increase the cost. Besides, the strong coupling between the control inputs and circuit status renders a high nonlinearity, which complicates the control design [40].

In order to address the aforementioned issues, a cascaded voltage control method is proposed in this paper. This control scheme allows the DC-link voltage to fluctuate within a wide range so that the F-cap, which is relatively more reliable, can be used for power buffering. Besides, the proposed control scheme can adaptively adjust the average DC-link voltage of ES for reducing the power loss of the passive circuit components, which can improve the efficiency and reliability of ES. The main contributions of this manuscript can be summarized as follows: (i) The quasi-steady-state (QSS) and steady-state (SS) operating models of the ES-based smart load are firstly developed for the concurrent control of smart load reactive power and average DC-link voltage. (ii) The optimum average DC-link voltage is mathematically derived according to the SS operating conditions. Such optimum average DC-link voltage will lead to the minimum power loss of the passive circuit components. (iii) An inner-loop model predictive voltage controller is designed for achieving the robust control of ES output voltage. The simulation and experiment results of 110 V AC microgrids have been provided to verify the performance and loss reduction capability of the proposed control scheme.

II. Limitations of Conventional Single-Phase ES

In this paper, unless otherwise noted, the lower-case variables with uppercase subscripts denote the combination of DC and AC signals, while the all-uppercase and all-lowercase variables denote pure DC and pure AC signals, respectively. Fig. 1 shows an ES-integrated AC microgrid. The power station has a tightly-regulated output voltage of v_g. It powers the AC microgrid through a distribution line with an impedance of Z_L. The RG (e.g., solar panels and wind turbines) are driven by the MPPT controller. They inject the intermittent current i_r to the grid, which disturbs the voltage v_m at the PCC. The NCL can tolerate a certain degree of variation on its supply voltage. Typically, it can be a thermal-electric load. The ES imposes a tunable voltage v_c between the PCC and the NCL. $|V_M|$ is the root-mean-square (RMS) value of v_m.

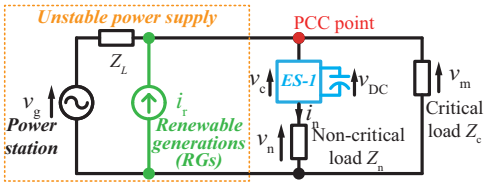
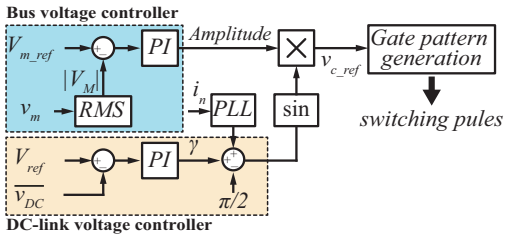
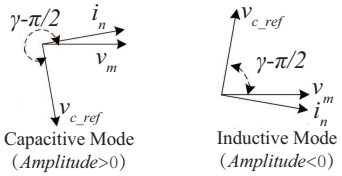


Fig. 1. An ES-integrated AC microgrid.



(a) The conventional linear control block diagram of ES [19]

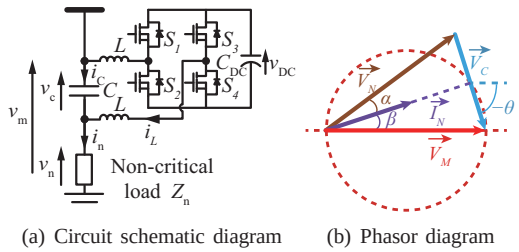


(b) Phasor diagram of ES

Fig. 2. The conventional linear control block diagram and phasor diagram of ES.

The conventional linear control block diagram of ES can be plotted as shown in Fig. 2(a). The modulated phase angle of v_c lags the phase angle of i_n by 90°. When $|V_M|$ is under-voltage ($V_{M\_ref} - |V_M| > 0$), a positive amplitude of v_{c_ref} will be generated. As shown in the left side of Fig. 2(b), the modulated v_c will eventually lag i_n by 90° and the ES will be operated in the capacitive mode. Similarly, when $|V_M|$ is over-voltage ($V_{M\_ref} - |V_M| < 0$), a negative amplitude of v_{c_ref} will be generated. As shown in the right side of Fig. 2(b), v_c will lead i_n by 90° and the ES will be operated in the inductive mode. In the mean time, the DC-link voltage controller will generate a correcting angle γ in the phase angle of v_{c_ref} to regulate the average DC-link voltage $\overline{v_{DC}}$ to the reference V_{ref}. As a result, the load pattern of NCL will automatically follow the fluctuating generation profile of RG and a stable PCC voltage can be provided for the CLs.

The circuit schematic diagram of the ES-based smart load is shown in Fig. 3(a). The ES is achieved by a full-bridge converter and the NCL is considered as a dissipative load with



(a) Circuit schematic diagram (b) Phasor diagram

Fig. 3. Circuit schematic diagram and phasor diagram of the ES-based smart load.

a constant impedance of $|Z_N|\angle\alpha$. The corresponding phasor diagram of the smart load can be plotted as shown in Fig. 3(b). The instantaneous power of ES can be expressed as

$$\begin{aligned} p_c &= 2|V_C||I_N|\cos(\omega t-\theta)\cos(\omega t+\beta) \\ &= |V_C||I_N|\cos(\theta+\beta)+|V_C||I_N|\cos(2\omega t+\beta-\theta) \\ &= P_C + p_{c2\omega}, \end{aligned} \tag{1}$$

where

$$\begin{cases} P_C = |V_C||I_N|\cos(\theta+\beta) \\ p_{c2\omega} = |V_C||I_N|\cos(2\omega t+\beta-\theta) \end{cases}. \tag{2}$$

In SS operation, $P_C \approx 0$ W. The ES has a double-line-frequency pulsating power of $p_{c2\omega}$, which will be buffered by the DC-link capacitor. For the conventional ES with E-cap, there are two defects, namely,

(i) Use of large DC-link capacitor. Generally, the E-cap demands small voltage ripples and v_{DC} can be approximated as $\overline{v_{DC}}$. By denoting η as the permissible voltage ripple in percentage, the requirement of DC-link capacitance can be expressed by

$$C_{DC} \geq \frac{|V_C||I_N|}{4\pi f \overline{v_{DC}{}^2}\eta}, \tag{3}$$

where f is the line frequency. Since the E-cap requires a small η, C_{DC} will be large.

(ii) Low efficiency. Conventionally, $\overline{v_{DC}}$ is controlled to be constantly-high for achieving the undistorted modulation of v_c. However, the operating point of ES is adaptively changed with respect to the variation of RG. The constantly-high $\overline{v_{DC}}$ will render low utilization of DC-link voltage and high voltage stress of the passive circuit components. This induces unnecessary power loss. As the power loss is mainly transformed into heat, the reliability and efficiency of ES may be degraded.

To improve the reliability and efficiency of ES, it is desirable to replace the E-cap with a relatively more reliable F-cap and adaptively operate $\overline{v_{DC}}$ for reducing the unnecessary power loss of ES. This new configuration brings several challenges in the design of ES voltage controller, namely,

(i) Robustness against the variation of DC-link voltage. By neglecting the power of the filtering components, it can be derived that

$$\begin{aligned} v_{DC}C_{DC}\frac{dv_{DC}}{dt} &= P_C + p_{c2\omega} \\ v_{DC} &= \sqrt{\overline{v_{DC}{}^2} + \frac{|V_C||I_N|\sin(2\omega t+\beta-\theta)}{\omega C_{DC}}}, \end{aligned} \tag{4}$$

where $\overline{v_{DC}{}^2}$ is the moving average of $v_{DC}{}^2$ over one-half line period. As the F-cap has a relatively smaller capacitance, v_{DC} will fluctuate at a larger range. Thus, the approximation of a constant v_{DC} is no longer valid for the conventional linear voltage controller of ES. A new control scheme, which is sufficiently robust to the variation of v_{DC}, is required for the control of v_c.

(ii) Adaptive control of average DC-link voltage. Considering v_c is adaptively changed with respect to the fluctuation of v_m, v_{DC} should be optimized with respect to the SS operating condition in a real-time manner for improving the utilization of DC-link voltage. On the one hand, $\overline{v_{DC}}$ shall be sufficiently low to reduce the power loss. On the other hand, $\overline{v_{DC}}$ must be properly controlled to ensure an undistorted modulation of v_c.

To address these challenges, a cascaded voltage control scheme is proposed for the voltage control of ES. The contents of this paper is organized as follows: In Section III, the QSS and SS models of smart load will be analyzed. Based on these models, the optimum average DC-link voltage of ES is derived in Section IV. The design of the cascaded controller will be elaborated in Section V. The experiment and simulation results are included in Section VI.

III. SS and QSS Models of the Smart Load

With respect to Fig. 3(b), the bus voltage and ES output voltage phasors can be expressed as $\vec{V_M} = |V_M|\angle 0°$ and $\vec{V_C} = |V_C|\angle(-\theta)$, respectively. The apparent power of ES and smart load can be derived by using

$$\begin{cases} S_C = P_C + jQ_C = |V_C|\angle(-\theta)\overline{\left[\frac{|V_M|\angle 0°-|V_C|\angle(-\theta)}{|Z_N|\angle\alpha}\right]} \\ S_M = P_M + jQ_M = |V_M|\angle 0°\overline{\left[\frac{|V_M|\angle 0°-|V_C|\angle(-\theta)}{|Z_N|\angle\alpha}\right]} \end{cases}, \tag{5}$$

where

$$\begin{cases} P_C = \dfrac{|V_M||V_C|\cos(\alpha-\theta)-|V_C|^2\cos\alpha}{|Z_N|} \\ Q_C = \dfrac{|V_M||V_C|\sin(\alpha-\theta)-|V_C|^2\sin\alpha}{|Z_N|} \\ P_M = \dfrac{|V_M|^2\cos\alpha-|V_M||V_C|\cos(\theta+\alpha)}{|Z_N|} \\ Q_M = \dfrac{|V_M|^2\sin\alpha-|V_M||V_C|\sin(\theta+\alpha)}{|Z_N|} \end{cases}. \tag{6}$$

Based on (6), the QSS operating model of smart load can be derived as

$$\begin{cases} (P_M-\dfrac{P_{max}}{2})^2+Q_M^2 = r_Q^2 \\ r_Q = \sqrt{\left(\dfrac{P_{max}}{2}\right)^2 - P_C P_{max}} \\ P_{max} = \dfrac{|V_M|^2}{|Z_N|\cos\alpha} \end{cases}, \tag{7}$$

where r_Q is defined as the QSS radius. P_{max} is the active power of NCL when the smart load is operated to achieve the unity power factor. The detailed derivations of (7) are elaborated in the Section VIII of Appendix. In QSS operation,

$P_C \neq 0$ W and $\overline{v_{DC}}$ will be adaptively changed. In SS operation, $P_C = 0$ W and $\overline{v_{DC}}$ will remain at a constant value. Hence, the SS operating model of smart load can be expressed as

$$\begin{cases} (P_M - \dfrac{P_{max}}{2})^2 + Q_M^2 = R_S^2 \\ R_S = \dfrac{P_{max}}{2} = \dfrac{|V_M|^2}{2|Z_N|\cos\alpha} \end{cases}, \tag{8}$$

where R_S is defined as the SS radius.

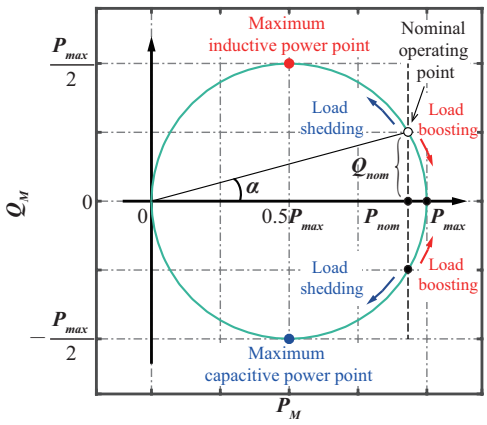


Fig. 4. Operating point of the ES-based smart load.

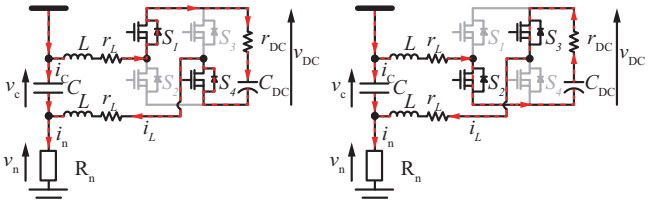
The operating point of the ES-based smart load can be plotted as shown in Fig. 4 according to (8). It is essentially a circle, which is centred at $(\frac{P_{max}}{2}, 0)$ and has a radius of $\frac{P_{max}}{2}$. When $\vec{V_C} = 0$ V, the smart load is operated at the nominal operating point of (P_{nom}, Q_{nom}), which can be expressed as

$$\begin{cases} P_{nom} = \dfrac{|V_M|^2\cos\alpha}{|Z_N|} \\ Q_{nom} = \dfrac{|V_M|^2\sin\alpha}{|Z_N|} \end{cases}. \tag{9}$$

The reactive power compensating capacity of the ES-based smart load is positively associated with the load capacity of NCL. When the smart load is operated at $(\frac{P_{max}}{2}, \frac{P_{max}}{2})$, it absorbs the maximum reactive power of $\frac{P_{max}}{2}$ Var from the grid. When the smart load is operated at $(\frac{P_{max}}{2}, -\frac{P_{max}}{2})$, it delivers the maximum reactive power of $\frac{P_{max}}{2}$ Var to the grid.

IV. Derivation of the Optimum DC-Link Voltage

The power loss on the passive components consists of the ohmic loss and the core loss. Here, the bipolar pulse width modulation scheme is applied and the switching states of the ES-based smart load are shown in Fig. 5.



(a) $S_{1,4}$ turned on and $S_{2,3}$ turned off. (b) $S_{2,3}$ turned on and $S_{1,4}$ turned off.

Fig. 5. Switching states of the ES-based smart load.

A. Ohmic Loss of Passive Components

In Fig. 5, r_L and r_{DC} are the equivalent series resistance (ESR) of the filtering inductors and DC-link capacitor, respectively. r_L and r_{DC} are at the same loop in every switching state. Thus, they can be equivalent to a resistor r, i.e.,

$$r = 2r_L + r_{DC}. \tag{10}$$

The ohmic loss of passive circuit components consists of the fundamental-frequency and switching-frequency components, which can be expressed as

$$P_{Loss} = P_f + P_{fsw} = r_f|I_F|^2 + r_{fsw}|I_{FSW}|^2. \tag{11}$$

In (11), r_f and r_{fsw} are the fundamental-frequency and switching-frequency equivalent resistance of r, respectively. $|I_F|$ is the RMS value of the fundamental inductor current, while $|I_{FSW}|$ is the RMS value of the switching ripples of the inductor current. At the fundamental frequency, the inductor current is approximately identical to the NCL current, i.e.,

$$|I_F| \approx |I_N|. \tag{12}$$

This means that P_f is determined by the SS operating point of the smart load. At the switching frequency, the RMS value of the inductor current ripple can be expressed as

$$|I_{FSW}| = \frac{1}{\sqrt{12}}\frac{(v_c - v_{DC})T_{sw}d}{2L}, \tag{13}$$

where T_{sw} is the average switching period. In the SS operation, the duty ratio can be expressed as

$$d = \frac{v_c + v_{DC}}{2v_{DC}}. \tag{14}$$

By combining (13) and (14), the switching-frequency ohmic loss of the passive circuit components can be expressed as

$$P_{fsw} = r_{fsw}|I_{FSW}|^2 = \frac{r_{fsw}(v_c^2 - v_{DC}^2)^2}{192L^2v_{DC}^2f_{sw}^2}, \tag{15}$$

where f_{sw} is the switching frequency. The profile of P_{fsw} can be plotted with respect to v_{DC} as shown in Fig. 6.

By solving the first-order differential function of $\frac{\partial P_{fsw}}{\partial v_{DC}} = 0$, the theoretical DC-link voltage v_{th}, which leads to the minimum P_{fsw}, can be expressed as

$$v_{th} = v_c. \tag{16}$$

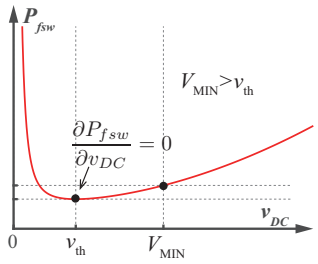


Fig. 6. Profile of switching-frequency ohmic loss.

B. Core Loss of Filtering Inductors

The core loss of the filtering inductors can be calculated by using the Steinmetz Equation of

$$P_{core} = 2C_m f^{\alpha} B^{\beta} A_c l_m, \tag{17}$$

where C_m, α and β are material parameters, f is the operating frequency, and B is the peak AC flux density. A_c and l_m denote the cross-section area and length of the magnetic core, respectively. According to Faraday's Law and (14), (17) can be rearranged as

$$\begin{aligned} P_{core} &= 2C_m f^{\alpha} \left[\frac{(v_{DC}-v_c)T_{sw}d}{NA_c}\right]^{\beta} A_c l_m \\ &= 2C_m f^{\alpha} \left[\frac{(v_{DC}^2-v_c^2)T_{sw}}{2v_{DC}NA_c}\right]^{\beta} A_c l_m, \end{aligned} \tag{18}$$

where N denotes the number of turns of the coil. Since $\frac{\partial P_{core}}{\partial v_{DC}} > 0$, it can be concluded that a smaller v_{DC} will render a smaller core loss. Ideally, the minimum P_{core} will be obtained when $v_{DC} = v_c$, which is the same with the theoretical results of (16).

C. Minimum DC-link Voltage Requirement

Besides, the average DC-link voltage must be sufficiently high to achieve the undistorted modulation of v_c. By neglecting the fundamental voltages across the filtering inductors, the waveforms of the v_{DC} and rectified v_c can be plotted as shown in Fig. 7.

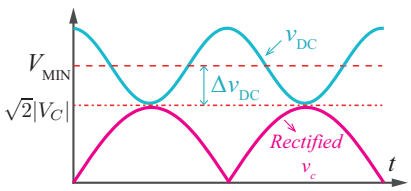


Fig. 7. Waveforms of v_{DC} and rectified v_c.

Considering the double-line-frequency voltage ripples on v_{DC}, the minimum value of $\overline{v_{DC}}$ can be expressed as

$$V_{MIN} = \sqrt{2}|V_C| + \Delta v_{DC}, \tag{19}$$

where Δv_{DC} is the amplitude of the voltage ripples. It can be derived by using

$$\begin{aligned} &\max\left(\int_{t_0}^{\frac{\pi}{2\omega}+t_0} p_{c2\omega}dt\right) \\ &\quad = \frac{1}{2}C_{DC}[(\overline{v_{DC}}+\Delta v_{DC})^2 - (\overline{v_{DC}}-\Delta v_{DC})^2] \\ &\Delta v_{DC} = \frac{|V_C||I_N|}{2\omega C_{DC}\overline{v_{DC}}}. \end{aligned} \tag{20}$$

By substituting (20) into (19), the minimum average DC-link voltage can be expressed as

$$V_{MIN} = \sqrt{2}|V_C| + \frac{|V_C||I_N|}{2\omega C_{DC}\overline{v_{DC}}}. \tag{21}$$

Obviously, $V_{MIN} > v_{th}$. By the convexity of Fig. 6, it is desirable to set $\overline{v_{DC}} = V_{MIN}$ to achieve the minimum P_{fsw} and P_{core}. By setting $\overline{v_{DC}} = V_{MIN}$ in (21), the optimum average DC-link voltage can be expressed as

$$V_{OPT} = V_{MIN} = \frac{\sqrt{2}|V_C|}{2} + \sqrt{\frac{|V_C|^2}{2} + \frac{|V_C||I_N|}{2\omega C_{DC}}}. \tag{22}$$

V. Design of Cascaded Voltage Controller

The overall block diagram of the proposed controller can be plotted as shown in Fig. 8. The cascaded voltage controller consists of an inner-loop voltage controller and an outer-loop voltage controller. The outer-loop voltage controller is applied to derive the voltage reference v_{c_ref} so that the corresponding optimum average DC-link voltage V_{OPT} and the desirable smart load reactive power Q_M can be concurrently achieved. The inner-loop voltage controller is used to isolate the variation of v_{DC} from propagating to v_c and achieve fast dynamic response of v_c.

As shown in Fig. 8, the PCC voltage error v_e is used to derive the reactive power reference Q_{M_ref}. The SS operating point and V_{OPT} will be derived according to the SS model. Then, the DC-link voltage controller will derive P_C with respect to V_{OPT}. At last, with the obtained P_C and Q_{M_ref}, v_{c_ref} will be calculated for the inner-loop voltage controller by using the QSS model.

A. Design of Outer-Loop Voltage Controller

According to the SS model expressed by (8), the desirable SS operating point can be derived by using

$$\begin{cases} Q_M = Q_{M\_ref},\ P_M = R_S + \sqrt{R_S^2 - Q_M^2} \\ |I_N|\angle\beta = \dfrac{P_M - jQ_M}{|V_M|\angle 0^\circ} \\ |V_C|\angle(-\theta) = |V_M|\angle 0^\circ - |Z_N||I_N|\angle(\alpha+\beta) \end{cases}. \tag{23}$$

With the calculated $|I_N|$ and $|V_C|$, V_{OPT} can be derived by using (22).

According to the power conservation of ES, it can be derived that

$$\begin{aligned} v_{DC}\frac{C_{DC}dv_{DC}}{dt} &= p_c - 2r{i_L}^2 - 2L\frac{di_L}{dt}i_L - C\frac{dv_c}{dt}v_c \\ \frac{d{v_{DC}}^2}{dt} &\approx \frac{2}{C_{DC}}(p_c - 2r{i_L}^2 - L\frac{d{i_L}^2}{dt}). \end{aligned} \tag{24}$$

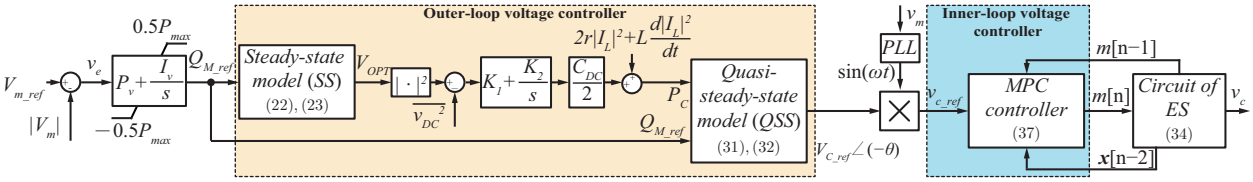


Fig. 8. Block diagram of the proposed cascaded voltage controller.

Considering C is very small, its power is neglected in (24). By averaging (24) over one-half line period, i.e.,

$$\begin{aligned} 2f\int_{t}^{t+\frac{1}{2f}}\left(\frac{dv_{DC}{}^2}{dt}\right)dt \\ = 2f\int_{t}^{t+\frac{1}{2f}}\frac{2}{C_{DC}}(p_c - 2ri_L{}^2 - L\frac{di_L{}^2}{dt})dt \\ \frac{d\overline{v_{DC}{}^2}}{dt} = \frac{2}{C_{DC}}(P_C - 2r|I_L|^2 - L\frac{d|I_L|^2}{dt}), \end{aligned} \tag{25}$$

the dynamics of $\overline{v_{DC}{}^2}$ can be derived. In (25), $|I_L|$ is the RMS value of the inductor current. $\overline{v_{DC}}$ can be regulated through controlling $\overline{v_{DC}{}^2}$. To compensate the error between $\overline{v_{DC}{}^2}$ and V_{OPT}^2, the control law of $\overline{v_{DC}{}^2}$ can be designed as

$$\frac{d\overline{v_{DC}{}^2}}{dt} = K_1 e_{DC} + K_2\int e_{DC}dt, \tag{26}$$

where

$$e_{DC} = V_{OPT}^2 - \overline{v_{DC}{}^2}. \tag{27}$$

Considering the change of V_{OPT}^2 is relatively slower than $\overline{v_{DC}{}^2}$, (26) can be approximated as

$$K_1 e_{DC} + K_2\int e_{DC}dt + \frac{de_{DC}}{dt} = 0. \tag{28}$$

As long as K_1 and K_2 are positive, e_{DC} will converge to 0. The control block diagram of $\overline{v_{DC}{}^2}$ can be plotted as shown in Fig. 9. By using the loop-shaping method, the value of K_1 and K_2 can be designed.

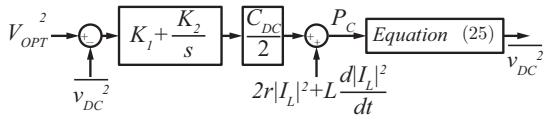


Fig. 9. Control block diagram of $\overline{v_{DC}{}^2}$.

With the calculated P_C and Q_{M_ref}, the intermediate QSS operating point of (P_I, Q_I) can be derived according to the QSS operating model. The QSS operating point of smart load can be plotted as shown in Fig. 10. As illustrated, when $r_Q \geq Q_{M\_ref}$,

$$\begin{cases} Q_I = Q_{M\_ref} \\ P_I = r_Q + \sqrt{r_Q^2 - Q_I^2} \end{cases}. \tag{29}$$

When $r_Q < Q_{M\_ref}$, the maximum achievable P_C will satisfy that

$$r_Q = \sqrt{\left(\frac{P_{max}}{2}\right)^2 - P_C P_{max}} = Q_I, \tag{30}$$

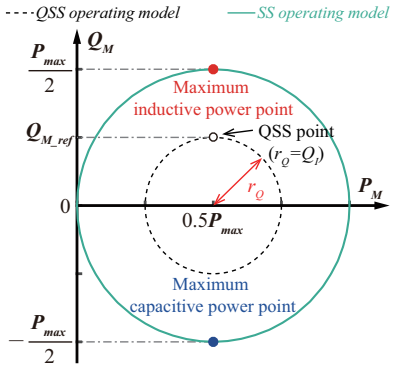


Fig. 10. QSS operating point of the smart load.

which makes $P_I = 0.5P_{max}$. To avoid the irrational solution of P_I, the desired intermediate QSS operating point can be expressed as

$$\begin{cases} Q_I = Q_{M\_ref} \\ P_I = 0.5P_{max} \end{cases} \tag{31}$$

Correspondingly, the ES output voltage reference can be calculated by using

$$|V_{C\_ref}|\angle(-\theta) = |V_M|\angle 0° - \frac{P_I - jQ_I}{|V_M|\angle 0°}|Z_N|\angle\alpha. \tag{32}$$

B. Design of Inner-Loop Voltage Controller

To reject the disturbance of v_{DC} without compromising the control bandwidth of v_c, the model predictive control (MPC) is applied and v_{DC} is fed back for the determination of control signals.

1) Discrete State-Space Model: For the ease of analysis, the NCL can be approximated as a resistive load R_n. The bipolar pulse width modulation scheme is applied to generate the switching pulses for switch S_x, where the subscript $x = \{1,\ 2,\ 3,\ 4\}$. S_1 and S_4 will be switched on and off simultaneously. By defining the duty ratio of S_1 and S_4 as d, the modulation index can be expressed as

$$m = 2d - 1. \tag{33}$$

By averaging the switching states shown in Fig. 5 in one switching period, the small-signal state-space model of smart load can be expressed as

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\cdot\boldsymbol{x} + \boldsymbol{B}\cdot\boldsymbol{u}$$

$$\begin{cases} \boldsymbol{A} = \begin{bmatrix} -\dfrac{1}{R_n C} & -\dfrac{1}{C} & 0 \\ \dfrac{1}{2L} & -\dfrac{r}{2L} & -\dfrac{m}{2L} \\ 0 & \dfrac{m}{C_{DC}} & 0 \end{bmatrix} \\ \boldsymbol{x} = [\widetilde{v_c},\ \widetilde{i_L},\ \widetilde{v_{DC}}]^T \\ \boldsymbol{B} = [\dfrac{1}{R_n C},\ 0,\ 0]^T \\ \boldsymbol{u} = [\widetilde{v_m}] \end{cases}, \tag{34}$$

where $|\dot{\cdot}|$ denotes the derivative of $|\cdot|$ and $\widetilde{|\cdot|}$ represents the small-signal component of $|\cdot|$.

As illustrated by (34), when the Forward Euler Approximation with a sampling period of T_s is applied, it takes two steps for the control effort of $m[n-1]$ to take effect on the output voltage, which leads to inaccurate control of v_c. To improve the accuracy of the prediction model, the state-space model of (34) is discretized at a sampling period of $\frac{T_s}{2}$. Assuming v_m remains constant in a period of T_s, the discrete state-space model of smart load with a sampling period of $\frac{T_s}{2}$ can be expressed as

$$\boldsymbol{x}[n] = \boldsymbol{A_d} \cdot \boldsymbol{x}[n-1] + \boldsymbol{B_d} \cdot \boldsymbol{u_d}$$

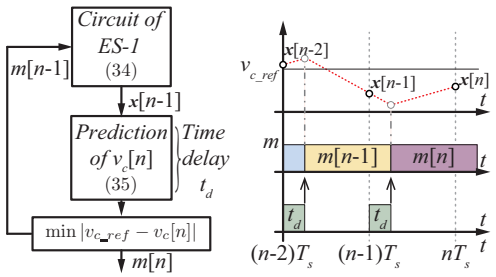
$$\begin{cases} \boldsymbol{A_d} = (\dfrac{T_s}{2}\boldsymbol{A} + \boldsymbol{I})^2 \\ \boldsymbol{x}[n-1] = [v_c[n-1],\ i_L[n-1],\ v_{DC}[n-1]]^T \\ \boldsymbol{B_d} = \left(\dfrac{T_s}{2}\right)^2 \boldsymbol{A} \cdot \boldsymbol{B} + T_s \boldsymbol{B} \\ \boldsymbol{u_d} = \boldsymbol{u} = [\widetilde{v_m}] \end{cases}. \tag{35}$$

2) Delay Compensation: With the measured information of $\boldsymbol{x}[n-1]$, the optimum control decision of $m[n]$ can be made by minimizing the error between the predicted $v_c[n]$ and v_{c_ref}, i.e.,

$$\begin{aligned} & \min |v_{c\_ref} - v_c[n]| \\ s.t.\quad & \boldsymbol{x}[n] = \boldsymbol{A_d} \cdot \boldsymbol{x}[n-1] + \boldsymbol{B_d} \cdot \boldsymbol{u_d} \\ & m[n] = \{-1,\ 1\}. \end{aligned} \tag{36}$$

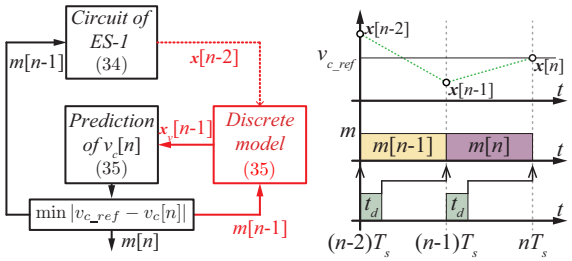
In the practical implementation of this MPC, it takes time for the digital signal processor (DSP) to predict all possible $v_c[n]$ as shown in Fig. 11(a). This results in a time delay of t_d between the measurement of $\boldsymbol{x}[n-1]$ and the execution of $m[n]$. The time sequence diagram of this MPC can be plotted as shown in Fig. 11(b). Since the sampling time point of $(n-1)T_s$, the circuit state vector has drifted away from the measured state vector of $\boldsymbol{x}[n-1]$. After t_d, the control signal of $m[n]$, which is calculated according to $\boldsymbol{x}[n-1]$, is executed. Consequently, this delayed execution of $m[n]$ will lead to a SS error between $v_c[n]$ and v_{c_ref}.

In order to compensate this SS error, a virtual measurement of $\boldsymbol{x_v}$ is introduced in the feedback loop of the MPC. As shown in Fig. 12(a), the actual measurement of $\boldsymbol{x}[n-1]$ is replaced by $\boldsymbol{x_v}[n-1]$ in the prediction of $v_c[n]$. $\boldsymbol{x_v}[n-1]$ is calculated according to the previous measurement of $\boldsymbol{x}[n-2]$, the previous control signal of $m[n-1]$ and the discrete state-space model of (35). Thus, the original output voltage MPC



(a) Control block diagram (b) Time sequence diagram

Fig. 11. Illustrations of time-delay-uncompensated MPC.



(a) Control block diagram (b) Time sequence diagram

Fig. 12. Illustrations of time-delay-compensated MPC.

of (36) can be reformulated as

$$\begin{aligned} & \min |v_{c\_ref} - v_c[n]| \\ s.t.\quad & \boldsymbol{x}[n] = \boldsymbol{A_d} \cdot \boldsymbol{x_v}[n-1] + \boldsymbol{B_d} \cdot \boldsymbol{u_d} \\ & \boldsymbol{x_v}[n-1] = \boldsymbol{A_d}\,|_{m=m[n-1]} \cdot \boldsymbol{x}[n-2] + \boldsymbol{B_d} \cdot \boldsymbol{u_d} \\ & m[n] = \{-1,\ 1\}. \end{aligned} \tag{37}$$

In this way, the prediction of $v_c[n]$ can be conducted one period ahead of time, i.e., before the time point of (n-1)th sampling. As shown in Fig. 12(b), this leaves a time margin of T_s for the DSP to predict $v_c[n]$. Thus, the desirable $m[n]$ can be derived in advance and be executed right at the (n-1)th sampling.

VI. Experiment and Simulation Results

TABLE I
Specifications of Experiment Setup

Description	Parameter	Value
Referenced bus voltage	$\|V_M\|$	110 V
Line impedance	Z_L	$(1+6.28\text{j})\ \Omega$
IGBT switches	$S_{1,2,3,4}$	IRG4PC30FDPBF
Filtering capacitor	C	1 μF
F-cap (B32526T3156K000)	C_{DC}	15 μF
E-cap (UBT2E680MHD +UBT2E470MHD)	C_{DC}	115 μF
Filtering inductor	L	3.3 mH
ESR of filtering inductor	r_L	0.3 Ω
NCL	Z_N	110 Ω
MPC sampling frequency	T_s	40 kHz
DSP controller		TMS320F28069

In this section, three experiments and one simulation have been performed. The experiment setup is shown in Fig. 13 and its circuit schematic diagram is shown in Fig. 3(a). A Chroma programmable AC source 61511 is applied to emulate

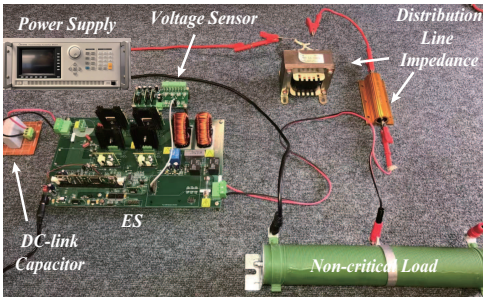
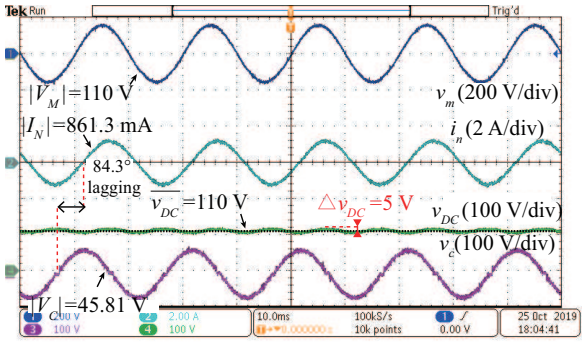


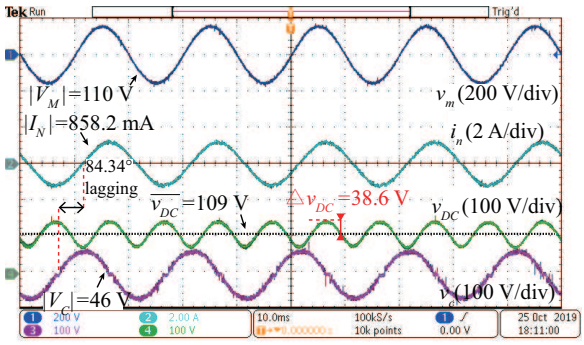
Fig. 13. Experiment setup of the ES-based smart load.

the unstable power supply. An impedance with an X/R ratio of 6.3 is used for emulating the impedance of distribution line. The corresponding specifications are summarized in Table I. In the first experiment, the SS operation of ES is demonstrated to verify the robustness of the inner-loop voltage controller against the variation of v_{DC}. The second experiment is conducted to compare the transient responses of ES with the proposed and conventional voltage control schemes. The third experiment is performed to verify the loss reduction ability of the proposed controller at different SS operating points. At last, a simulation is conducted to demonstrate the loss reduction ability of the proposed controller in the real-time compensation of fluctuating powers.

A. SS Operations



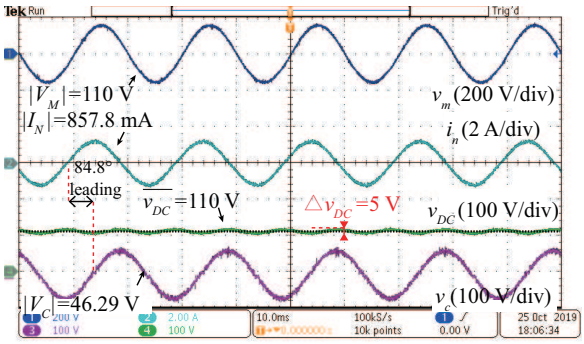
(a) $Q_{M\_ref} = 40$ Var, $C_{DC} = 115$ μF.



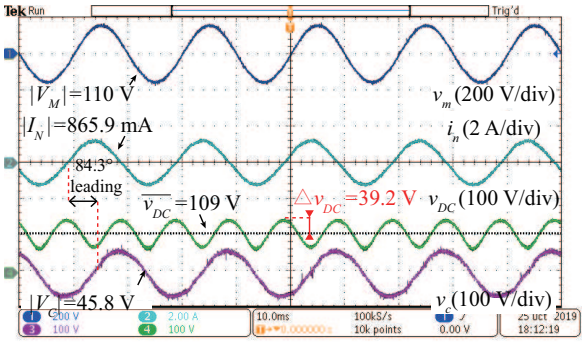
(b) $Q_{M\_ref} = 40$ Var, $C_{DC} = 15$ μF.

Fig. 14. Experiment waveforms of smart load in inductive operations.

In this experiment, the ES with E-cap is controlled by the conventional linear voltage controller to provide the referenced



(a) $Q_{M\_ref} = -40$ Var, $C_{DC} = 115$ μF.



(b) $Q_{M\_ref} = -40$ Var, $C_{DC} = 15$ μF.

Fig. 15. Experiment waveforms of smart load in capacitive operations.

reactive powers, while the ES with F-cap is controlled by the proposed voltage controller to achieve the same reactive power compensation. By setting $\eta = 5\%$ and $\overline{v_{DC}} = 110$ V, the minimum required E-cap can be calculated as 105 μF according to (3). Here, the capacitance of E-cap is set to 115 μF for a conservative design. For the ES with F-cap, the DC-link capacitance is set to 15 μF.

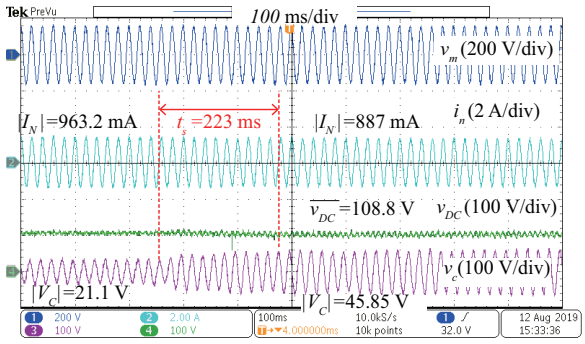
When the supply voltage is set at 114.4 V, Q_{M_ref} will be controlled to be 40 Var to suppress the bus voltage from 113 V to 110 V. When the bus voltage is stabilized, the AC source is delivering an active power of 90.3 W and a reactive power of 45.4 Var to the loads. As shown in Fig. 14(a) and 14(b), i_n lags v_c by 84.3° and $|V_C|$ is controlled to be 45.8 V. The smart load is absorbing a reactive power of 39.3 Var from the grid. For the ES with E-cap, $\overline{v_{DC}}$ is controlled at 110 V and v_{DC} is fluctuating at an amplitude of 5 V. For the ES with F-cap, $\overline{v_{DC}}$ is controlled at 109 V. The DC-link ripple voltage has an amplitude of 38.6 V, which is 35.4% of $\overline{v_{DC}}$.

When the supply voltage is set at 108.5 V, Q_{M_ref} will be controlled to be -40 Var to boost the bus voltage from 107.4 V to 110 V. When the bus voltage is stabilized, the AC source has an active power of 90 W and a reactive power of -36 Var. As shown in Fig. 15(a) and 15(b), v_c leads i_n by 84.8° and $|V_C|$ is controlled to be 46 V. The smart load is delivering a reactive power of 39.6 Var to the system. For the ES with E-cap, $\overline{v_{DC}}$ is stabilized at 110 V and Δv_{DC} is 5 V. For the ES with F-cap, $\overline{v_{DC}}$ is controlled at 109 V. Δv_{DC} is 39.2 V, which is 36% of $\overline{v_{DC}}$.

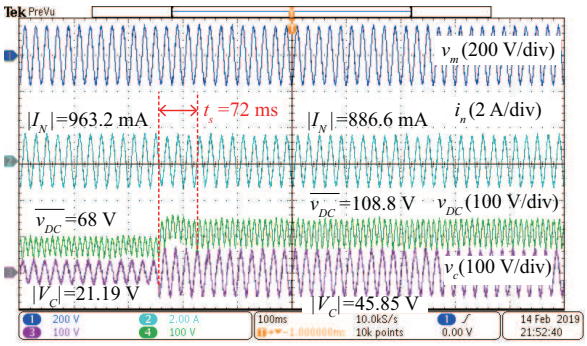
By comparing the waveforms of v_c shown in Fig. 14(a) and 15(a) with that of Fig. 14(b) and 15(b), it can be seen that the

proposed controller can achieve the undistorted modulation of v_c against the significant variation of v_{DC} in both the inductive and capacitive operations of the ES. By referring to the datasheets of the F-cap [41] and E-cap [42], the lifetime of the applied F-cap is 200000 h, which is 100 times of the lifetime of the adopted E-cap. This proves that the reliability of the ES can be significantly improved by using the F-cap as the DC-link capacitor.

B. Transient Responses of ES



(a) Conventional controller, $C_{DC} = 115\ \mu$F

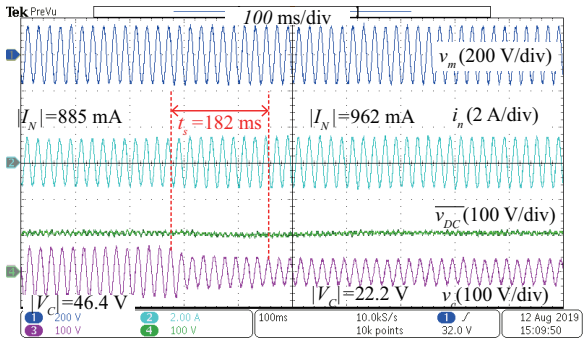


(b) Proposed controller, $C_{DC} = 15\ \mu$F

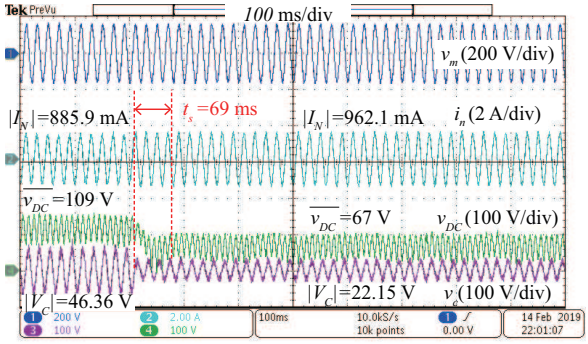
Fig. 16. Experiment waveforms of smart load stepping from 20 Var to 40 Var.

In this experiment, the supply voltage is firstly stepped from 114.4 V to 113.4 V then from 108.5 V to 110.4 V. Without activating the ES, $|V_M|$ will be stepped from 113.2 V to 112.2 V then from 107.35 V to 109.23 V. With the conventional and proposed control schemes, the reactive power of ES will be controlled from 20 Var to 40 Var then from -40 Var to -20 Var for restoring the PCC voltage to 110 V. For the ES with the F-cap (15 μF), the proposed cascaded voltage controller will operate the ES to achieve the desired reactive power references and regulate $\overline{v_{DC}}$ to the corresponding optimum values, simultaneously. For the ES with the E-cap, the conventional controller will control the ES to deliver the reactive power for restoring the bus voltage and $\overline{v_{DC}}$ will be regulated to a constant value of 110 V.

The transient waveforms of ES stepping from 20 Var to 40 Var are shown in Fig. 16. When the supply voltage is changed from 114.4 V to 113.4 V, the ES voltage $|V_C|$ will be operated from 21.1 V to 45.9 V in inductive mode for restoring $|V_M|$ to 110 V. As shown in Fig. 16(a), when the conventional controller is applied, it takes 223 ms for the ES to be settled at the referenced SS operating point. Meanwhile, $\overline{v_{DC}}$ is consistently controlled at 108.8 V. When the proposed controller is applied, the settling time is around 72 ms as shown in Fig. 16(b), which is significantly shorter than that of the conventional controller. In this step-change transient, $\overline{v_{DC}}$ is increased from 68 V to 108.8 V, which are close to the theoretical optimum references of 64.5 V and 104.8 V, respectively.



(a) Conventional controller, $C_{DC} = 115\ \mu$F



(b) Proposed controller, $C_{DC} = 15\ \mu$F

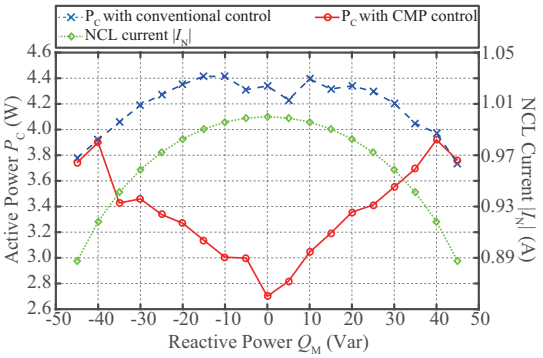
Fig. 17. Experiment waveforms of smart load stepping from -40 Var to -20 Var.

Fig. 17 illustrates the transient waveforms of ES stepping from -40 Var to -20 Var. In this step-change transient, the ES voltage will be changed from 46.4 V to 22.2 V in capacitive mode for boosting $|V_M|$ to 110 V. As shown in Fig. 17(a), when the conventional controller is applied, the measured settling time is 182 ms, which is larger than that of the ES with the proposed controller (69 ms). As shown in Fig. 17(b), $\overline{v_{DC}}$ is decreased from 109 V to 67 V during this transient, which are close to the theoretical optimum values of 104.8 V and 64.5 V.

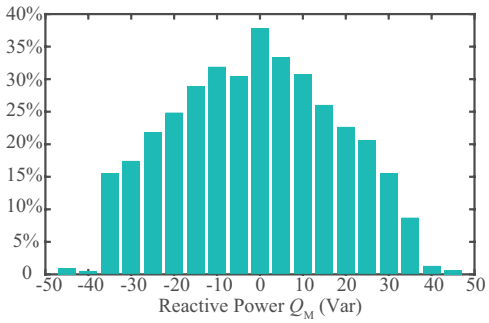
As illustrated in Fig. 16(b) and 17(b), the envelopes of the waveforms of v_{DC} are right above the profiles of v_c under the same voltage reference and scale. This ensures the undistorted modulation of v_c and reduces the voltage stress of the ES. The proposed controller can achieve the concurrent control of the smart load reactive power and average DC-link voltage. Besides, the proposed controller can enable a faster transient response of the ES-based smart load.

C. Reduction of ES Active Powers

In this experiment, Q_{M_ref} is gradually changed from -45 Var to 45 Var. The conventional constant DC-link voltage control scheme and the proposed cascaded voltage controller are respectively applied on ES to provide the same referenced reactive power. For the conventional control scheme, $\overline{v_{DC}}$ is consistently controlled at 110 V for all operating points. For the proposed controller, $\overline{v_{DC}}$ is adaptively adjusted according to (22). A YOKOGAWA power analyzer WT1806E is used to measure the active power of ES at different SS operating points.



(a) Measured active powers and currents of ES



(b) Reduced active power of ES in percentage with the proposed controller

Fig. 18. Measured active powers and reduced active powers of ES with respect to Q_M.

As shown in Fig. 18(a), the measured active powers and currents of ES are plotted with respect to the measured reactive powers. When the conventional controller is applied, the measured active power is decreased with respect to the increase of compensated reactive power capacity $|Q_M|$. As illustrated by the green curve of Fig. 18(a), the inductive and capacitive operations of ES will shed the NCL and reduce $|I_N|$. As I_N is reduced, the current stress of the passive circuit components is alleviated and the power loss will be reduced. The real powers of ES with the proposed cascaded controller are generally smaller than the cases of the conventional controller. This verifies that the proposed control scheme can effectively reduce the power loss of ES. The reduced active power of ES in percentage with the proposed cascaded control scheme can be plotted as shown in Fig. 18(b). When Q_M is close to 0 Var, the reduced active power is significant. While Q_M is close to -45 Var and 45 Var, the reduced active power is small. This is because that, when $|Q_M|$ is small, the ES with conventional control scheme has a low utilization of the DC-link voltage, which renders unnecessary voltage stress and extra power loss. With the proposed cascaded control scheme, $\overline{v_{DC}}$ is adaptively changed with respect to v_c for improving the utilization of v_{DC}. Therefore, the power loss of the ES can be effectively reduced.

D. Compensation of Fluctuating Powers in AC Microgrids

TABLE II
SPECIFICATIONS OF SIMULATION SETUP

Description	Parameter	Value
Source voltage	$\|V_G\|$	$109.3 \sim 114.2$ V
Source active power	P_S	3288 W$\sim$ 4018 W
Line impedance	Z_L	$(0.043 + 0.3\text{j})\ \Omega$
Source reactive power	Q_S	-951 Var$\sim$ 836 Var
Filtering capacitor	C	$1\ \mu$F
DC-link capacitor	C_{DC}	$1000\ \mu$F
ESR of DC-link capacitor	r_{DC}	$2\ \text{m}\Omega$
Filtering inductor	L	3.3 mH
ESR of filtering inductor	r_L	$30\ \text{m}\Omega$
NCL	Z_N	$6.05\ \Omega$
CL	Z_C	$6.05\ \Omega$
Average switching frequency	f_{sw}	20 kHz

In this simulation, the ES is operated to compensate the power fluctuations in a 110 V AC microgrid. The circuit schematic of the microgrid is shown in Fig. 1 and the specifications of corresponding parameters are listed in Table II. As the ES is generally applied in distribution grid, the X/R ratio of Z_L is set to be 7 to simulate the impedance of the distribution line [15], [43]. The unstable power supply generates fluctuating powers to the loads, which disturbs $|V_M|$. The time profile of the generated active power (see Fig. 20(a)) fluctuates between 3.3 kW and 4 kW, while the curve of the generated reactive power (see Fig. 20(b)) varies between -951 Var and 836 Var. The ES is controlled to restore $|V_M|$ to 110 V with the conventional controller and the proposed controller, respectively. The simulation is conducted for 200 s and the corresponding simulated time profiles are shown in Fig. 19, 20(a), 20(b), 20(c) and 20(d).

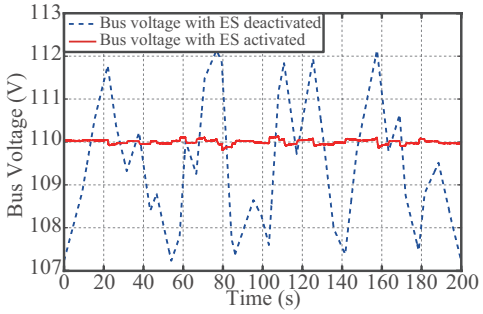
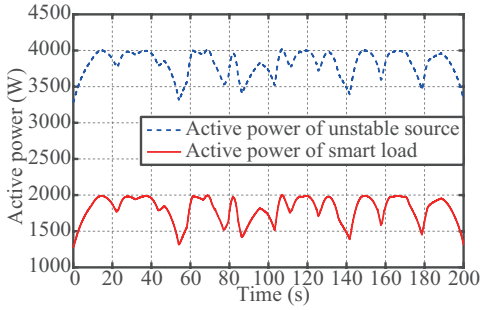
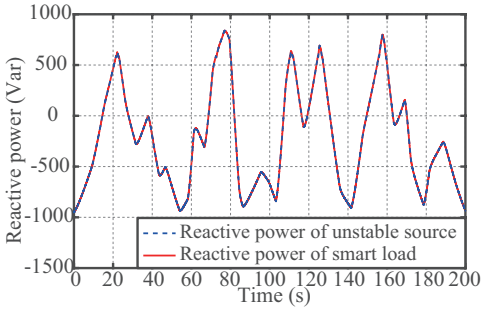


Fig. 19. AC bus voltage with and without activating ES.

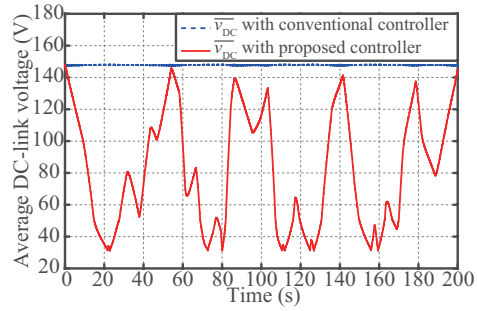
In this simulation, the voltage of the supply voltage is controlled to fluctuate between 109.3 V and 114.2 V to simulate the intermittency of the unstable source. As illustrated in Fig. 19, without activating the ES, the RMS value of the PCC voltage is varying between 107.3 V and 112.2 V. When



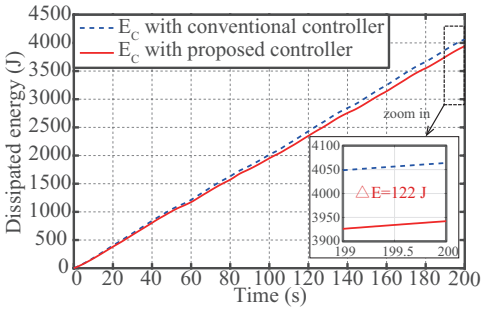
(a) Time profiles of generated active power and smart load real power.



(b) Time profiles of generated reactive power and smart load reactive power.



(c) Time profiles of average DC-link voltage.



(d) Time profiles of the cumulative dissipated energy of ES.

Fig. 20. Simulated waveforms of ES compensating the fluctuating powers in AC microgrids.

the ES is activated, V_M is regulated to 110 V and the bus voltage is stabilized.

The profiles of the generated active power and the smart load real power are shown in Fig. 20(a). The pattern of the smart load active power is similar to the profile of the source active power. This means that the smart load is operated to consume the unstable part of the generated active power. Fig. 20(b) illustrates the time profiles of the generated reactive powers and smart load reactive power. The profile of the smart loads reactive power overlaps the profile of generated source reactive power. This proves that the smart load can effectively compensate the reactive power fluctuations of the unstable source.

Fig. 20(c) shows the time profiles of $\overline{v_{DC}}$ with the conventional and the proposed controllers. For ES with the conventional controller, $\overline{v_{DC}}$ is consistently regulated at 148 V. For ES with the proposed controller, $\overline{v_{DC}}$ is adaptively changed between 31 V and 148 V. At the beginning and the ending time points of this simulation, $\overline{v_{DC}}$ is deliberately controlled at 148 V so that the accumulated energy of ES are solely dissipated as power loss. The time profiles of the cumulative dissipated energy of ES with two types of controllers are shown in Fig. 20(d). After 200 s, the accumulated energy dissipation of ES with the proposed controller is 3929 J, which is 3% smaller than the case of the conventional controller (4064 J). This proves that the proposed cascaded control scheme can effectively reduce the power loss of ES in the real-time operation of compensating grid power fluctuations.

VII. Conclusions

The ES can effectively address the intermittency of RG with its ability of manipulating NCL in a real-time manner. To improve the reliability and efficiency of the ES, the cascaded voltage control scheme is proposed for the ES with DC-link film capacitor. Both the SS and QSS operating models of ES are developed for the accurate derivation of ES output voltage reference. Mathematical derivations of the optimum average DC-link voltage for achieving the minimum power loss are provided. It is illustrated that by operating the average DC-link voltage of ES at a properly low level, the power loss of ES can be effectively reduced. The robust inner-loop voltage controller is designed to isolate the disturbance of v_{DC} from propagating to the output without dampening the transient response of v_c. By applying the inner-loop voltage controller, a small F-cap (15 μF) can be used to replace the large E-cap (115 μF) as the DC-link capacitor without deteriorating the ES outputs. The experimental and simulation results have verified that the proposed control scheme can effectively improve the efficiency and reliability of ES.

VIII. Appendix

When the smart load is operated at the unity power factor, the smart load active power can be calculated by using

$$P_{max} = \frac{|V_M|^2}{|Z_N| \cos \alpha} \tag{38}$$

By combining (6) and (38), the QSS model can be derived as

$$
\begin{aligned}
&(P_M - 0.5P_{max})^2 + Q_M^2 \\
&= \left[\underbrace{\frac{|V_M|^2\cos\alpha - |V_M||V_C|\cos(\alpha+\theta)}{|Z_N|}}_{P_M} - \underbrace{\frac{|V_M|^2}{2|Z_N|\cos\alpha}}_{0.5P_{max}}\right]^2 \\
&\quad + \left[\underbrace{\frac{|V_M|^2\sin\alpha - |V_M||V_C|\sin(\alpha+\theta)}{|Z_N|}}_{Q_M}\right]^2 \\
&= \left(\frac{|V_M|^2}{2|Z_N|\cos\alpha}\right)^2 - \frac{|V_M|^4\cos\alpha - |V_M|^3|V_C|\cos(\alpha+\theta)}{|Z_N|^2\cos\alpha} \\
&\quad + \frac{|V_M|^4(\cos^2\alpha+\sin^2\alpha) + |V_M|^2|V_C|^2}{|Z_N|^2} \\
&\quad - \frac{2|V_M|^3|V_C|\left[\cos(\alpha+\theta)\cos\alpha + \sin(\alpha+\theta)\sin\alpha\right]}{|Z_N|^2} \\
&= \left(\frac{|V_M|^2}{2|Z_N|\cos\alpha}\right)^2 - \frac{|V_M|^4\cos\alpha - |V_M|^3|V_C|\cos(\alpha+\theta)}{|Z_N|^2\cos\alpha} \\
&\quad + \frac{|V_M|^4 + |V_M|^2|V_C|^2 - 2|V_M|^3|V_C|\cos\theta}{|Z_N|^2} \\
&= \underbrace{\left(\frac{|V_M|^2}{2|Z_N|\cos\alpha}\right)^2}_{0.5\mathrm{P_{max}}} \\
&\quad + \underbrace{\frac{|V_C|^2\cos\alpha - |V_M||V_C|\cos(\alpha-\theta)}{|Z_N|}}_{-\mathrm{P_C}} \times \underbrace{\frac{|V_M|^2}{|Z_N|\cos\alpha}}_{\mathrm{P_{max}}} \\
&= \left(\frac{P_{\max}}{2}\right)^2 - P_C P_{\max}.
\end{aligned}
\tag{39}
$$

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