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Bias Stress Stability Improvement in Solution-processed Low-voltage Organic Field-effect Transistors Using Relaxor Ferroelectric Polymer Gate Dielectric

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***Abstract*—Low voltage organic field effect transistors (OFETs) using relaxor ferroelectric polymer poly(vinylidene fluoridetrifluoroethylene-chlorofloroethylene) (P(VDF-TrFE-CFE)) were fabricated. The measured hysteresis loop and threshold voltage shift under negative bias stress (NBS) are opposite to that of the reference device using low-*k* CYTOP gate dielectric layer, in which the hysteresis and NBS induced instabilities are explained by gate bias induced charge trapping. The anomalous behaviors in the P(VDF-TrFE-CFE) OFETs are attributed to the stress-induced remnant polarization in P(VDF-TrFE-CFE), which induces additional mobile charges into the channel. By adding a thin CYTOP layer between the P(VDF-TrFE-CFE) layer and the semiconductor layer, the two effects of charge trapping and remnant polarization under gate bias are found to be neutralized with each other, resulting in low voltage OFETs of negligible hysteresis and excellent NBS stability.**

***Index Terms*—organic field-effect transistor (OFET), low voltage, solution processed, high-*k*.**

I. Introduction

Being processed by solution or printing based approaches at low temperature, and owing excellent intrinsic mechanical flexibility, organic field-effect transistors (OFETs) will find a wide range of applications in low-cost and flexible electronics especially displays, sensors and hybrid integration systems [1-3]. However, for those envisioned practical applications, reducing the operation voltage and improving the operational stability under electrical bias becomes the major challenges. Enlarging the gate dielectric capacitance for enhanced gate control of the channel is a widely adopted approach for low voltage OFETs. It can also be helpful in improving the current driving capability and the transconductance, and minimizing possible short-channel effects with shorter channel devices [4]. High gate capacitance can be achieved by using a ultra-thin gate dielectric layer. However, in the fabrication of OFETs over large area substrates with solution based or printing processes, this approach is not applicable due to the resulted poor device reliability and low yield. Therefore, lots of work has been carried out on using high dielectric constant (high-*k*) gate dielectric material for low voltage OFETs [5]. To meet the overall needs of low temperature solution processing and intrinsic mechanical flexibility of OFETs, polymer high-*k* dielectrics are more preferable, compared to inorganic counterparts. Among very few choices of high-*k* polymer dielectrics, relaxor ferroelectric polymer poly(vinylidene fluoridetrifluoroethylene-chlorofloroethylene) (P(VDF-TrFE-CFE)) was reported to have the highest *k* value of about 60 [6], and has been successfully used in low-voltage OFETs based on various organic semiconductors[7-9]. However, the operational stability under bias stress with OFETs using this gate dielectric layer has not been studied. , It has been reported that a negative gate bias stress (NBS) can induce a threshold voltage (V_{th}) shift in a p-type OFET operated in inert environment [10]. The main mechanism for the NBS induced V_{th} shift is attributed to be the trapping of carriers from the gate bias-induced conduction channel into less mobile localized states. Therefore, V_{th} of the device normally shifts toward the negative direction [11]. In this work, we found that p-type OTFTs with the P(VDF-TrFE-CFE) high-k gate dielectric under continuous NBS shows V_{th} shift towards the positive direction., By inserting a thin CYTOP layer between the P(VDF-TrFE-CFE) layer and the semiconductor layer, we luckily found that the NBS stability as well as the overall performance of the device was significantly improved due to the synergic effect of the double-layer gate dielectric.

II. Experimental

The OFETs were fabricated with a top-gate bottom-contact structure as shown in Fig. 1. The fabrication details can be

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found in [12]. Chromium (Cr) of 5 nm and gold (Au) of 40 nm were thermally evaporated onto pre-cleaned glass substrate through a shadow mask to define source/drain (S/D) electrodes with the channel width of 2000 μm and channel length of 120 μm. The surfaces of the S/D electrodes were treated with pentafluorobenzenethiol (PFBT) self-assembled monolayers (SAMs) to form better contacts with the organic semiconductor layer. Donor-acceptor copolymer semiconductor indacenodithiophene-benzothiadiazole (IDTBT) was deposited by spin-coating from a 5 mg/ml solution in chlorobenzene, followed by annealing at 150 ℃ for 30 min in nitrogen (N_2) atmosphere. A 270 nm thick P(VDF-TrFE-CFE) gate dielectric layer was formed by spin-coating a 40 mg/ml P(VDF-TrFE-CFE) solution (56/36.5/7.5 mol%) in methyl ethyl ketone and subsequently annealing at 65 ℃ for 3 hours in N_2 atmosphere. A reference device was fabricated using an about 900 nm thick CYTOP gate dielectric layer, deposited by spin-coating of the CYTOP solution (CTL-809M, Asahi Glass Japan) as received and annealing in vacuum at 100 ℃ for 30 min. The thin layer CYTOP of about 8 nm thickness inserted between the P(VDF-TrFE-CFE) layer and the IDTBT layer was formed by spin-coating a diluted CYTOP solution dissolved in its solvent CT-Solv.180 in a ratio of 1:30 (wt%). Finally, for all three type devices, 100 nm-thick aluminum (Al) gate electrodes were deposited by thermal evaporation. All the electrical characterization was carried out with a Agilent 4156C semiconductor parameter analyzer in N_2 atmosphere to exclude any influence from water and oxygen in the air ambient. The capacitances were characterized with an Agilent 4294A precision impedance analyzer at 40 Hz. The measured k values of P(VDF-TrFE-CFE) and CYTOP are about 58 and 2.1, respectively.

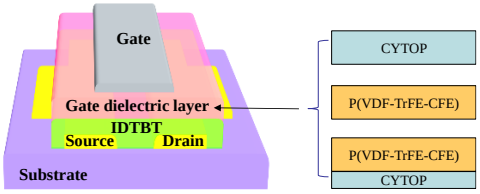

Fig. 1. Schematic of the device structure of the top-gate bottom-contact OFET to be studied in this work using different gate dielectric layers: single layer CYTOP, single layer relaxor ferroelectric terpolymer P(VDF-TrFE-CFE), and P(VDF-TrFE-CFE)/CYTOP bilayer.

III. Results and Discussions

Fig. 2 (a) and (b) show the measured forward and reverse transfer curves (I_D-V_{GS}) for the fabricated OFETs using CYTOP and P(VDF-TrFE-CFE) as the gate dielectric layer, respectively. Compared to the CYTOP device with subthreshold swing (*SS*) of 2.1 V/dec, the P(VDF-TrFE-CFE) one has much smaller *SS* of 150 mV/decade attributed to the large gate dielectric capacitance of 190 nF/cm^2. The mobility reduction from about 1.3 cm^2/V·s for the CYTOP device to 0.3 cm^2/V·s for the P(VDF-TrFE-CFE) one is caused by enhanced carrier localization due to the random dipoles at the surface of the high-k gate dielectric, which has been discussed previously [12-13].

For the CYTOP device, the hysteresis loop in Fig. 2(a) is along the clockwise direction, while for the P(VDF-TrFE-CFE) device, it is along the anti-clockwise direction (Fig. 2(b)). The hysteresis windows for both devices are about 0.5 V as indicated. The I_D-V_{GS} curves measured at different time under continuous NBS for the two type devices are given in Fig. 2(c) and (d), respectively. It can be seen that the I_D-V_{GS} curve of the CYTOP device shifts towards the negative direction, and differently, the I_D-V_{GS} curve of the P(VDF-TrFE-CFE) one shifts towards the positive direction. The hysteresis and NBS instability behaviors of the CYTOP device can be explained by gate bias induced trapping of positive charges into localized states [14], which, however, is obviously not applicable to the P(VDF-TrFE-CFE) device.

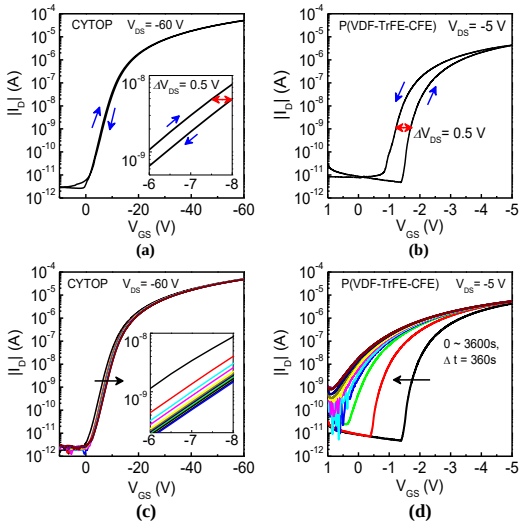

Fig. 2. (a) The measured forward and reverse transfer curves (I_D-V_{GS}) for the OFET with CYTOP gate dielectric layer. (b) The measured forward and reverse I_D-V_{GS} for the OFET with P(VDF-TrFE-CFE) gate dielectric layer. (c) I_D-V_{GS} curves measured at different time under negative bias stress (NBS) at V_{GS}= -60 V, V_{DS}= -5 V for the CYTOP OFET. (d) I_D-V_{GS} curves measured at different time during NBS at V_{GS}= -5 V, V_{DS}= -0.5 V for the P(VDF-TrFE-CFE) OFET.

Such a high k value of 58 with P(VDF-TrFE-CFE) is formed by large dipole moment of the monomer unit, high dipole density and strong dipolar coupling between the polarization entities in the VDF structure [7]. Although its polarization induced hysteresis is much reduced by introducing CFE units to prohibit the formation of large polarization domains, the remnant polarization cannot be completely eliminated [6, 7]. Previous work has also provided direct experimental evidence of electric field induced polarization in the ferroelectric relaxor terpolymer [15, 16]. Therefore, when P(VDF-TrFE-CFE) directly interfaces the organic semiconductor layer, dipole electric field caused by this remnant polarization under gate bias will induce additional mobile charges in the channel [17]. As a result, it leads to higher channel current, and thus the anti-clockwise hysteresis loop and also positive shift of I_D-V_{GS} curve under NBS.

For the CYTOP/P(VDF-TrFE-CFE) OFET, both the hysteresis and NBS induced I_D-V_{GS} shift become negligible as shown in Fig. 3(a) and (b), respectively. The device can still be operated below 5 V with a gate dielectric capacitance of 104 nF/cm^2, despite of a slightly larger *SS* of 158 mV/dec. The

mobility is about 1.3 $cm^2/V{\cdot}s$, similar to that of the CYTOP device. The extracted threshold voltage (V_{th}) shifts over time under NBS for the three type devices are compared in Fig. 3(c). V_{th} of the P(VDF-TrFE-CFE) device and the CYTOP one shifts towards the opposite directions due to the different mechanisms as discussed above. The CYTOP/P(VDF-TrFE-CFE) device has much improved bias stress stability with V_{th} less than 0.08 V after 3600 s. These results indicate that in the CYTOP/P(VDF-TrFE-CFE) device the two effects of charge trapping and remnant polarization under gate bias are neutralized with each other. To further prove this, the drain current evolution over time for the three devices under continuous NBS were plotted in Fig.3(d). It can be seen that the current decay with the CYTOP device fits very well with the following equation (1) in a stretched exponential law standing for charge trapping effect [18].

$$I_D(t) = I_D(0)exp\left[-\left(\frac{t}{\tau_d}\right)^{\beta}\right] \quad (1)$$

where $I_D(0)$ is the initial drain current, τ_d the characteristic time for charge trapping, and β the dispersion parameter. In contrast to the CYTOP device, the drain current for the P(VDF-TrFE-CFE) device increases rapidly in the beginning and then reached a maximum value, which agrees well with the following equation (2) describing the current evolution over time under gate bias due to polarization effect [18]

$$I_D(t) = I_D(0) + \Delta I_D(\infty)\left\{1 - exp\left[-\left(\frac{t}{\tau_p}\right)^{\alpha}\right]\right\} \quad (2)$$

where $\Delta I_D(\infty)$ is the constant current parameter, τ_p the characteristic time for polarization, and α the dispersion parameter.

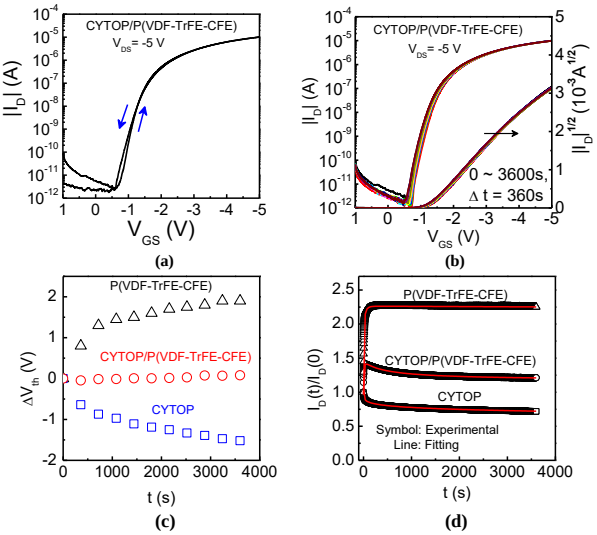

Fig. 3. (a) The measured forward and reverse transfer curves (I_D-V_{GS}) for the fabricated OFET with CYTOP/P(VDF-TrFE-CFE) bilayer gate dielectric. (b) I_D-V_{GS} curves measured at different time under negative bias stress (NBS) at V_{GS}= -5V, V_{DS}= -0.5 V for the bilayer OFET. (c) Comparisons of the extracted threshold voltage (V_{th}) shift over time under NBS for the three type OFETs with different gate dielectrics. (d) Comparisons of the drain current evolution over time for the three devices under continuous NBS.

The CYTOP/P(VDF-TrFE-CFE) device exhibits a current change which can be fit well using the following equation (3) as a sum of equation (1) and (2). The results prove that the combined effects of charge trapping and remnant polarization on improving the bias stress stabilities of the devices.

$$I_D(t) = \Delta I_D(\infty)\left\{1 - exp\left[-\left(\frac{t}{\tau_p}\right)^{\alpha}\right]\right\} + I_D(0)exp\left[-\left(\frac{t}{\tau_d}\right)^{\beta}\right] \quad (3)$$

IV. Conclusions

The fabricated low voltage OFETs using high-*k* P(VDF-TrFE-CFE) gate dielectric presents hysteresis loop and V_{th} shift under NBS opposite to that of the reference device with low-*k* CYTOP gate dielectric layer. The physical mechanism is considered to be that the dipole electric field from remnant polarization in P(VDF-TrFE-CFE) induces additional mobile charges into the channel. By adding a thin CYTOP layer between the P(VDF-TrFE-CFE) layer and the semiconductor layer, the two effects of charge trapping and remnant polarization under gate bias are found to be neutralized with each other, resulting in low voltage OFETs of negligible hysteresis and excellent NBS stability. This work provides a solution for developing low voltage and stable OFETs by using the high-*k* relaxor ferroelectric polymer as the gate dielectric layer.

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