A ferroelectric relaxor polymer-enhanced p-type WSe_2 transistor

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Abstract

WSe_2 has attracted extensive attention for p-FETs due to its air stability and high mobility. However, the Fermi level of WSe_2 is close to the middle of the band gap, which will induce a high contact resistance with metals and thus limit the field effect mobility. In this case, a high work voltage is always required to achieve a large ON/OFF ratio. Herein, a stable WSe_2 p-doping technique of coating using a ferroelectric relaxor polymer P(VDF-TrFE-CFE) is proposed. Unlike other doping methods, P(VDF-TrFE-CFE) not only can modify the Fermi level of WSe_2 but can also act as a high-*k* gate dielectric in an FET. Dramatic enhancement of the field effect hole mobility from 27 to 170 $cm^2 V^{-1} s^{-1}$ on a six-layer WSe_2 FET has been achieved. Moreover, an FET device based on bilayer WSe_2 with P(VDF-TrFE-CFE) as the top gate dielectric is fabricated, which exhibits high p-type performance over a low top gate voltage range. Furthermore, low-temperature experiments reveal the influence of the phase transition of P(VDF-TrFE-CFE) on the channel carrier density and mobility. With a decrease in temperature, field effect hole mobility increases and approaches up to 900 $cm^2 V^{-1} s^{-1}$ at 200 K. The combination of the p-doping and gating with P(VDF-TrFE-CFE) provides a promising solution for obtaining high-performance p-FET with 2D semiconductors.

1. Introduction

With current silicon devices approaching their limits, various emerging semiconductor materials, such as one-dimensional nanowires[1,2] and carbon nanotubes[3,4] and two-dimensional graphene[5,6] and transition metal dichalcogenides (TMDs),[7,8] have been proposed to replace silicon as channel materials. Due to its zero band gap, graphene faces a large challenge in digital electronic applications.[9–11] On the other hand, TMDs have a controllable bandgap, high mobility, and atomic scale size, which make it one of the most promising channel materials for the next-generation nanoelectronics.[12–14] Most of the TMDs, such as MoS_2, which have been studied widely, can form low electron barrier contact with metals and are generally used for n-type field-effect transistors (FETs).[15–18] Since both n-type and p-type transistors are the building blocks in complementary metal–oxide-semiconductor (CMOS) or diode technology, p-type channel materials are also highly required while integrating TMD-based CMOS logic or other devices based on pn-junction. $MoTe_2$ and two-dimensional (2D) black phosphorus have shown p-type properties according to the previous reports.[19–21] However, these materials are less stable under ambient conditions.

A more air-stable material WSe_2 has attracted extensive attention for p-FETs, and an early study on bulk-WSe_2 FETs reveals a high intrinsic hole mobility of 500 $cm^2\ V^{-1}\ s^{-1}$ but with a low ON/OFF ratio.[22] More recently, 2D WSe_2 FETs have been reported with a high hole mobility, high ON/OFF ratio, and layer-dependent bandgap ranging from indirect 1.2 eV to direct 1.6 eV.[23–26] In addition, the carrier type of WSe_2 can change from n-type to p-type when the thickness decreases from more than ten nanometers to several nanometers.[27] Moreover, contact metals with different work functions determine the channel type of WSe_2 FETs. For low-work function metals, such as aluminum (Al), silver (Ag), and indium (In),[28] the few-layer WSe_2 FETs show n-type behavior. On the other hand, they exhibit p-type behavior with high-work function metals such as platinum (Pt) and palladium (Pd).[29,30] However, the Fermi level of WSe_2 is close to the middle of the bandgap;[31] this makes it difficult to form low-resistance contact with metals and thus limits the field effect mobility, and high working voltage is usually required to achieve a large ON/OFF ratio. p-Doping is an effective way to make the Fermi level close to the valence band and lower the hole injection barrier with contact metals. At present, NO_2 chemical doping,[30] solid-state oxide doping,[27] gold decoration,[32] and

octadecyltrichlorosilane (OTS) interface dipole introduction[33] have been reported to achieve a p-doping effect on the WSe_2 channel and obviously increase the hole mobility. However, stability, process complexity, and doping density control are still challenges to be resolved in practical applications. Another way to enhance the performance of WSe_2 FETs is using high-*k* or a thinner dielectric layer to replace the traditional SiO_2.[30,34] A high-*k* or a thinner dielectric layer can generate higher charge density with a lower voltage according to the capacitance calculation formula and thus lower the power consumption of the FETs.

2D materials combined with a ferroelectric polymer have been proven to show better performance of FET devices.[35–38] Compared with the normal ferroelectric copolymer poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)), the terpolymer poly(vinylidene fluoride-trifluoroethylene-chlorofluoroethylene) (P(VDF-TrFE-CFE)) demonstrates typical relaxor ferroelectricity with a very small polarization but a high dielectric constant at room temperature;[39,40] this means it has great advantages for a gate dielectric.[41,42]

In this study, we demonstrated a p-doping technique on bilayer and six-layer WSe_2 flakes by coating them with P(VDF-TrFE-CFE). Carbon–fluorine (C–F) and carbon–chlorine (C–Cl) dipoles in P(VDF-TrFE-CFE) apply negative Poles onto the WSe_2 surface and consequently induce hole accumulation on WSe_2 and lower the Fermi level of WSe_2. Because P(VDF-TrFE-CFE) is covering WSe_2, it can isolate WSe_2 from ambient conditions and thus provide a stable and nondegenerate p-doping of the WSe_2 channel. After P(VDF-TrFE-CFE) coating, the field effect hole mobility derived under SiO_2 gating is enhanced from 27 to 170 $cm^2\ V^{-1}\ s^{-1}$, and the threshold voltage (V_{th}) has a positive shift from −41 V to −29 V (ΔV_{th} = +12 V). Unlike other doping methods, P(VDF-TrFE-CFE) not only can play the doping role by modifying the Femi level of adjacent semiconductors but can also act as a dielectric layer in FET. Gated by P(VDF-TrFE-CFE), the bilayer WSe_2 FET at room temperature shows a high ON/OFF ratio exceeding 2×10^7 in a narrow gate voltage range and a low off subthreshold swing (SS_{off}) of 175 mV dec^{-1}. Furthermore, the low temperature experiment displays a hysteresis conversion of the transfer curve because of the phase transition of the P(VDF-TrFE-CFE) from relaxor to ferroelectric. With a decrease in temperature, field effect hole mobility increases and approaches up to 900 $cm^2\ V^{-1}\ s^{-1}$ at 200 K.

2. Results and discussion

Fig. 1a shows the atomic force microscopy (AFM) image and optical microscope image of a bilayer WSe_2 flake placed on top of a Si/SiO_2 (SiO_2, thickness: 300 nm) substrate. The height profile of a line scan across the WSe_2–SiO_2 boundary shows that the thickness of WSe_2 is ~1.7 nm. It is about twice the thickness of the single layer WSe_2 (~0.7 nm),[30] such that this WSe_2 flake can be determined to be a bilayer. The height profile also shows a preferable flatness, which is essential for obtaining a high carrier mobility with low surface roughness scattering rates. The Raman spectrum of the bilayer WSe_2 is shown in Fig. 1b, and the atomic displacements of optical modes are shown in the inset. The most prominent two Raman peaks for the bilayer WSe_2 are the in-plane vibration mode (E^1_{2g}) and out-of-plane vibration mode (A_{1g}) located at 249.4 cm^{-1} and 250.9 cm^{-1}, respectively. The frequency difference between two peaks is 1.5 cm^{-1}, which is consistent with the recent experimental results.[43] Moreover, these two peaks are in agreement with previous calculations,[44] revealing both E^1_{2g} and A_{1g} modes close to 250 cm^{-1}. The three-dimension (3D) schematic of the bilayer WSe_2 FET gated by the P(VDF-TrFE-CFE) relaxor film (thickness, 200 nm) is shown in Fig. 1c. Moreover, the optical microscopy image of the device is shown in Fig. 1d. Pd is used as the contact metal, which will result in a higher channel current and hole mobility (Fig. S1 in the ESI†).

The molecular configurations of P(VDF-TrFE-CFE) in relaxed and ferroelectric states are shown in Fig. 2a. It is believed that the termonomer CFE serves as a local defect to the polarization ordering in the crystalline regions, which converts the all-*trans* (*TT*) polar conformation in the ferroelectric copolymer P(VDF-TrFE) to a relaxor terpolymer with a mixture conformations of polar phase ($T_{>3}G$), relaxor phase with polar nanoregion (T_3GT_3G), nonpolar *trans-gauche* ($TGTG'$), and paraelectric phase (TG_3TG_3).[45] The crystallinity and the polar and nonpolar regions, which are mainly related to temperature, can dramatically affect the property of the terpolymer P(VDF-TrFE-CFE). When the temperature is up to 340 K, the terpolymer is paraelectric with $TGTG'$ and TG_3TG_3 as the predominant phases. At room temperature, T_3GT_3G is the dominant phase, which makes P(VDF-TrFE-CFE) a relaxor, whereas it tends to be ferroelectric below 260 K because the $T_{>3}G$ phase starts to be superior over others.[45,46] The dielectric constant of P(VDF-TrFE-CFE) exhibits a strong dependence on temperature, as shown in Fig. 2b. Note that the dielectric constant has a broad peak around room temperature, and the peak shifts to a higher temperature for higher frequencies. Fig. 2c shows the ferroelectric hysteresis loops of the 200 nm P(VDF-TrFE-CFE) film capacitor at different

temperatures. The typical ferroelectric hysteresis loops obviously occur below 260 K, indicating that the film begins to transform from relaxor to ferroelectric. Transfer characteristic curves of the FET based on the bilayer WSe_2 channel driven by the P(VDF-TrFE-CFE) ferroelectric polymer top gate and SiO_2 back gate at room temperature are shown in Fig. 2d. Since P(VDF-TrFE-CFE) has a much higher dielectric constant (~55) than SiO_2 (~3.9) at room temperature, it can induce a much higher charge density of WSe_2 under the same gate voltage. Therefore, the device gated by P(VDF-TrFE-CFE) shows much better transfer characteristic with a low off-current below 10 pA, small SS ~175 mV dec^{-1}, and large ON/OFF ratio exceeding 2×10^7 within ± 10 V gate voltage. The inset of Fig. 2d also shows that the maximum field effect hole mobility with top gate voltage is 86.7 $cm^2\ V^{-1}\ s^{-1}$, and the unsaturated field effect hole mobility with back gate voltage is 9.2 $cm^2\ V^{-1}\ s^{-1}$. The field effect mobility is calculated using the following equation:[15]

$$\mu = \frac{dI_{ds}}{dV_g} \times \frac{L}{W} \times \frac{d}{\varepsilon_0 \varepsilon_r V_{ds}}$$

where dI_{ds}/dV_g is the slope of the I_{ds}–V_g curve, L and W are the length and width of the channel, d and ε_r are the thickness and dielectric constant of the dielectric layer, respectively, and ε_0 is the permittivity of vacuum, which is equal to 8.854×10^{-12} F m^{-1}.

Fig. 3a shows the transfer and output curves of a bilayer WSe_2 channel gated by SiO_2 before and after annealing at 200 °C under an argon atmosphere for 2 hours. With a large gate voltage, the transfer curve shows obvious anticlockwise hysteresis behavior, which is related to the surrounding conditions and charge trapping with surface defects.[47] After annealing, the ON current is enhanced approximately five times. The resistances calculated from the output curve before and after annealing are 235 MΩ and 91 MΩ, respectively. This resistance consists of two parts: WSe_2 channel resistance and contact resistance. Herein, the decrease in the resistance (ΔR = 145 MΩ) is mostly attributed to the reduction of the contact resistances since the channel resistance remains unchanged under the same gate voltage and channel interface condition. This proves that the proper annealing process has a positive effect on improving the contact. Fig. 3b and c show the transfer characteristic curves of a six-layer WSe_2 channel gated by SiO_2 before and after coating with P(VDF-TrFE-CFE) along with the output and mobility curves. The AFM image of this six-layer WSe_2 and optical image of the device are shown in Fig. S2.† According

to these transfer characteristic curves, a p-doping phenomenon can be found after coating with P(VDF-TrFE-CFE). As a result, the WSe_2 channel changed from slight bipolar to complete p-type after coating with P(VDF-TrFE-CFE). Moreover, a positive shift in threshold voltage (V_{th}) from −41 V to −29 V (ΔV_{th} = +12 V) was observed. More importantly, the ON current was increased ten-fold from 2.76×10^{-6} A to 2.59×10^{-5} A, and the field effect mobility was improved from 27.2 to 170.9 $cm^2\ V^{-1}\ s^{-1}$. This p-doping phenomenon is a common phenomenon that has also been observed in a bilayer WSe_2 channel after coating with P(VDF-TrFE-CFE), as shown in Fig. S3.† The p-doping effect is also observed in P(VDF-TrFE) on the $MoTe_2$ and WSe_2 channel according to a recent research.[37] Earlier studies have also shown that P(VDF-TrFE) can suppress n-type characteristics on a black phosphorus channel.[38] However, since P(VDF-TrFE) is ferroelectric at room temperature, the polarization of P(VDF-TrFE) may sometimes surpass the doping effect. The p-doping effect of P(VDF-TrFE) may not be as stable as that of P(VDF-TrFE-CFE). Fig. 3d shows the schematic of the band structure between WSe_2 and the Pd contact metal. The carrier type of the FETs based on 2D materials is substantially determined by the relative energy difference between the metal work function and the semiconductor conduction-band minimum (CBM) and valence-band maximum (VBM).[28,34,48] Generally, the WSe_2 channel tends to form a lower hole barrier rather than the electron barrier when in contact with high-work function metals. However, since the Fermi level of WSe_2 is close to the middle of the band gap, the channel still has a large hole barrier ($\Phi_{Bp} = E_p$) even in contact with Pd whose Fermi level is lower than the VBM of WSe_2 as shown in Fig. 3e. The positive shift of threshold voltage indicates that a higher hole concentration is induced at the same gate voltage. We believe that this higher hole concentration is derived from the charge induced by the electric dipole effect of the C–F and C–Cl bonds in P(VDF-TrFE-CFE). After coating with P(VDF-TrFE-CFE), the C–F and C–Cl dipoles in P(VDF-TrFE-CFE) make negative Poles onto the WSe_2 surface and consequently induce hole accumulation on WSe_2 and lower the Fermi level of WSe_2. Therefore, it reduces the hole injection barrier ($\Phi'_{Bp} = E'_p$) with Pd as the contact metal, as shown in Fig. 3f; this enhances the p-type property of FET. Unlike the NO_2 chemical doping method that showed a serious degeneration with time,[30] the technology proposed herein by coating with P(VDF-TrFE-CFE) achieved a stable, nondegenerate p-doping of the WSe_2 channel, as shown in Fig. S4.† Moreover, P(VDF-TrFE-CFE) is coated right on top of WSe_2, which can

isolate WSe_2 from the ambient conditions and introduce long-term effective p-doping interface dipoles.

To further investigate the property of the WSe_2 FET gated by P(VDF-TrFE-CFE), the transfer characteristic of the top gate device at various temperatures has been measured. Fig. 4a and b show the top gate transfer curves of a bilayer WSe_2 FET at temperatures around the Curie temperature ($T_c \sim 260$ K). With a decrease in temperature from 300 K to 260 K, all transfer curves show anticlockwise hysteresis, which can be ascribed to charge trapping by the surface defects.[47] In this case, as the temperature is reduced, more P(VDF-TrFE-CFE) tends to transfer from *TGTG′* and TG_3TG_3 phases to the T_3GT_3G phase, which is the ferroelectric phase. Therefore, the hysteresis window in the transfer curve becomes narrow with the decreasing temperature; this is opposite to the ferroelectric hysteresis loops of the P(VDF-TrFE-CFE), as shown in Fig. 2c. The shift of the on and off threshold voltage $V_{th\text{-}on}$ and $V_{th\text{-}off}$ in these transfer curves can also reflect the change of the hysteresis window, as shown in Fig. S5a.† $V_{th\text{-}off}$ and $V_{th\text{-}on}$ coincide and are equal to 0 V at 260 K, revealing that the competition between impurities and polar nanoregions achieve a balance. The coincident transfer curve and near-zero threshold voltage indicate the FET turning on and off by an ultra-low gate voltage. With a further decrease in temperature to below 260 K, P(VDF-TrFE-CFE) tends to be ferroelectric with the $T_{>3}G$ polar phase being dominant. The top gate transfer curve converts to clockwise hysteresis alone with the phase transition of P(VDF-TrFE-CFE), and the window becomes broader with a temperature decrease. The off subthreshold swing SS_{off} remains at a low value (~175 mV dec^{-1}) with the changing temperature, whereas the on subthreshold swing SS_{on} exhibits a significant decrease during the phase transition of the P(VDF-TrFE-CFE), as shown in Fig. S5b.† When the external gate voltage is swept from positive to negative, the hole concentration in WSe_2 is insufficient to compensate for the internal field induced by the P(VDF-TrFE-CFE), and the drain current increases slowly. By contrast, the hole concentration is abundant and can change rapidly to compensate for the internal field as the external gate voltage is swept from negative to positive; consequently, the SS_{off} is considerably smaller than the SS_{on}. When the temperature is decreased to below 260 K, P(VDF-TrFE-CFE) tends to be ferroelectric, and the decrease of SS_{on} may be derived from the ferroelectric negative capacitance (NC) effect during the polarization of ferroelectric domain switching.[49] The ferroelectricity of P(VDF-TrFE-CFE) at the ferroelectric

phase can be separated into three states: fresh state (without polarization), polarization (P) up state (polarized by $V_{tg} = -20$ V), and P down state (polarized by $V_{tg} = 20$ V). Fig. 4c shows the output curves without an external gate voltage under these three states of P(VDF-TrFE-CFE) at 200 K. The remanent polarization of P(VDF-TrFE-CFE) shows a distinct effect on the WSe_2 channel. In the P down state, the polarization of the ferroelectric layer suppresses the channel current to a great degree. It reveals a potential application in the photodetector because the polarized electric field can greatly suppress the dark current and enhance the photoresponsivity of the device even without a gate voltage.[36] Fig. 4d displays the temperature dependence of the field effect hole mobility for the FET gated by P(VDF-TrFE-CFE). The result agrees with the theoretical study indicating that the relationship between mobility and temperature follows an exponential law of $\mu \propto T^{-\gamma}$, where γ is a parameter depending on the phonon type in carrier-phonon scattering.[50] For 2D materials, acoustic phonon scattering is expected to result in $\gamma = 1$, whereas $\gamma > 1$ is a signature of optical phonon scattering being the dominant scattering mechanism.[50,51] Upon fitting with our experimental data, it was found that the value of γ was ~5.9. This high value demonstrates that the primary scattering mechanism is not only optical phonon scattering but also Coulomb scattering caused by the charge impurities induced by the dipoles of P(VDF-TrFE-CFE) and the SiO_2 substrate. Moreover, a high contact resistance should be taken into consideration. Fig. 4e and f illustrate the influence of P(VDF-TrFE-CFE) transition on channel carrier density. When the temperature is higher than T_c and the top gate voltage starts from negative, holes in WSe_2 are slowly trapped into the trap centers. The trapped holes do not participate in charge transport, but just act as a positive charge. Consequently, WSe_2 has a more positive potential in region R1 than that in R2 of Fig. 4a; thus, the channel current in R1 is smaller than that in R2 although these regions are in the same gate voltage. When the temperature decreases to below 260 K, P(VDF-TrFE-CFE) tends to be ferroelectric. At this time, when the top gate voltage starts from negative, the ferroelectric is polarized to be P up state and the impact of charge trapping is totally surpassed by the remanent polarization of the ferroelectric (and *vice versa* for the opposite sweep direction). Therefore, the channel currents in R3 is much higher than that in R4 (Fig. 4b), and the transfer curve turns into clockwise hysteresis.

The comparison of electrical performance of WSe_2-based FETs by several treatments at room temperature is shown in Table 1. It can be observed that the combined effect of p-doping and gating with P(VDF-TrFE-CFE) results in a high electrical performance in the WSe_2 FET.

3. Conclusion

A simple and stable p-doping technique for 2D WSe_2 by coating with a relaxor ferroelectric polymer, P(VDF-TrFE-CFE), is proposed. This p-doping phenomenon, including a positive V_{th} shift, ON current, and hole mobility enhancement, is thought to originate from the fact that C–F and C–Cl dipoles in P(VDF-TrFE-CFE) apply negative Poles onto the WSe_2 surface and consequently induce hole accumulation on WSe_2 and further lower the Fermi level of WSe_2. The effect of P(VDF-TrFE-CFE) as a high-*k* gate dielectric layer in bilayer WSe_2 FET has also been investigated. The WSe_2 channel is doped and gated by P(VDF-TrFE-CFE), which exhibits much better electrical performance than that driven by SiO_2. Furthermore, low-temperature experiments revealed the influence of the phase transition of P(VDF-TrFE-CFE) on the channel carrier density. A typical ferroelectric FET effect and high hole mobility were achieved at low temperatures. The combination of the p-doping and gating with P(VDF-TrFE-CFE) provides a new promising solution for obtaining a high-performance p-FET with 2D semiconductors.

4. Experimental

Back gate WSe_2 device fabrication

The few-layered WSe_2 was extracted by mechanical exfoliation of commercial WSe_2 bulk crystal and then transferred to a heavily doped p-type Si substrate covered with 300 nm thick SiO_2. The accurate number of layers of WSe_2 was confirmed by AFM. The electrodes of the devices were deposited by electron beam lithography technology, followed by thermal evaporation of the Pd/Au contact metals (10/40 nm thick). The devices were then annealed at 200 °C in vacuum under a 100 sccm argon atmosphere for 2 h to release the adsorbate and decrease the contact resistance.

Top gate WSe_2 device fabrication

Once the back gate device was fabricated and annealed, the P(VDF-TrFE-CFE) (56.2/36.3/7.5 mol%) organic ferroelectric polymer solution (dissolved in diethyl carbonate with 2.5 wt%) was spin coated on top of WSe_2 with a thickness of ~200 nm. Then, the P(VDF-TrFE-CFE) film was annealed at 118 °C under ambient conditions for 4 h. Finally, 10 nm thick aluminum was deposited on top of the P(VDF-TrFE-CFE) film by electron beam evaporation patterned by a shadow mask as the top-gate electrode.

Measurement

The electric properties of the device were measured by an Agilent B2902A semiconductor parameter analyzer in vacuum. The electric properties of the P(VDF-TrFE-CFE) were measured by Radiant precision LC ferroelectric tester by fabricating it into a plate capacitor structure. The temperature control system was cooled by vaporizing liquid nitrogen and heated by resistance heating silk with a temperature controller maintaining the temperature set point. Raman spectroscopy on the bilayer WSe_2 was carried out with 514.5 nm laser excitation.

Conflicts of interest

There are no conflicts of interest to declare.

Acknowledgements

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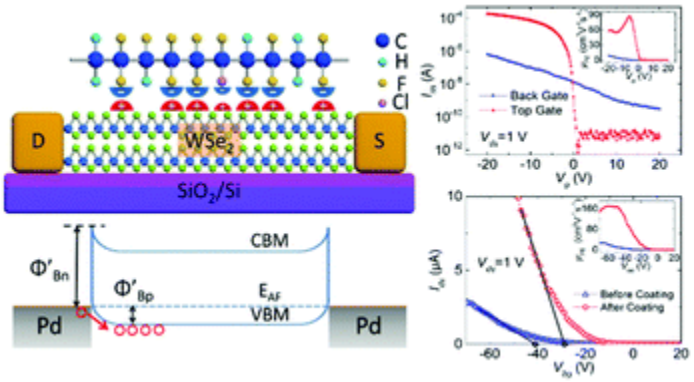
Graphical abstract



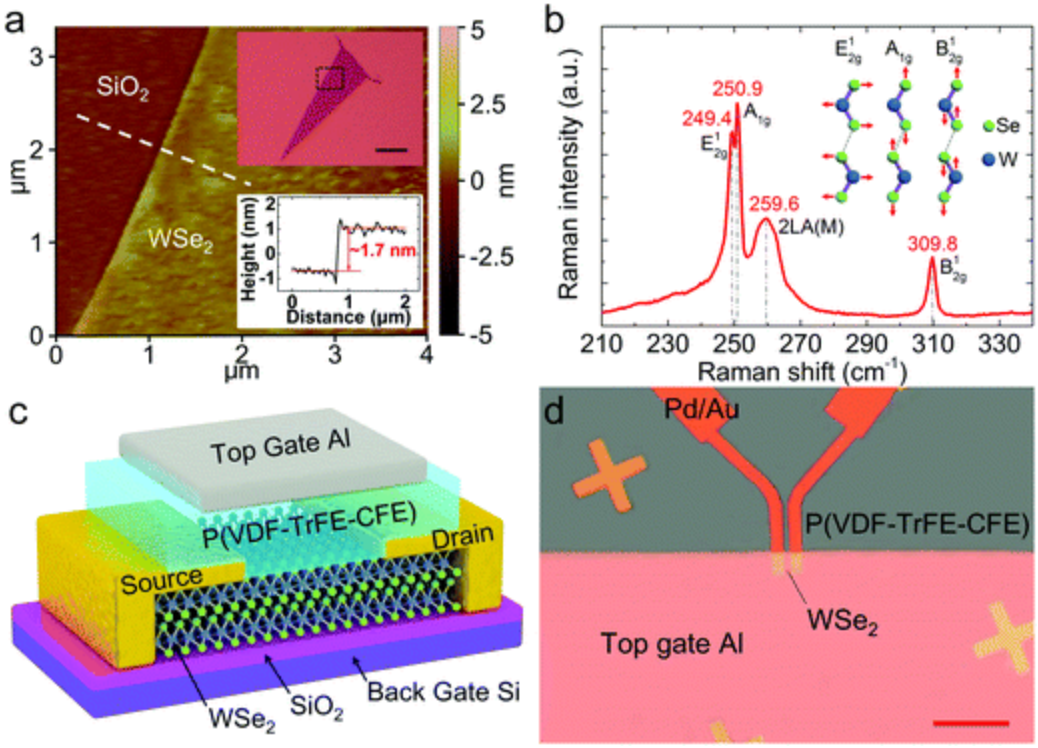


Fig. 1 Fabrication and structure of bilayer WSe_2 FET. (a) AFM image of a bilayer WSe_2 on Si/SiO_2 and insets show the optical microscopy image and height profile of a line scan across the WSe_2–SiO_2 boundary (dotted line), scale bar 5 μm. (b) Raman spectra of bilayer WSe_2 and atomic displacements for optical modes (inset). (c) 3D schematic of the bilayer WSe_2 FET driven by P(VDF-TrFE-CFE). (d) An optical microscopy image of the WSe_2 FET; the scale bar stands for 50 μm. The channel width is ~4 μm, length is ~5 μm, and the thickness of the P(VDF-TrFE-CFE) and SiO_2 is ~200 nm and ~300 nm, respectively.

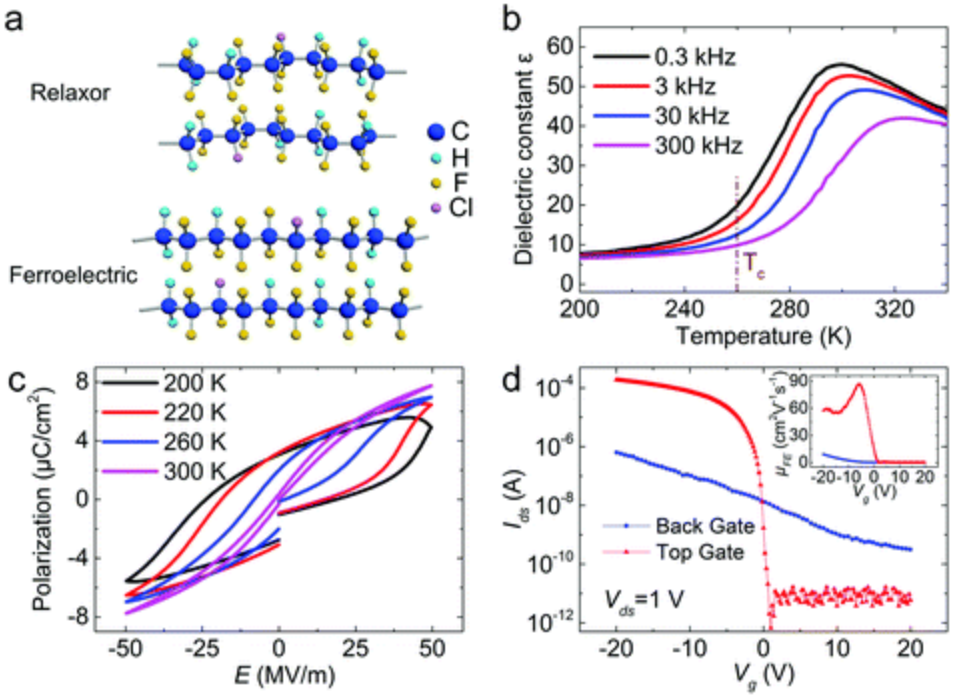


Fig. 2 Schematic structure of P(VDF-TrFE-CFE) and temperature-related electrical properties of the P(VDF-TrFE-CFE)/WSe_2 structure. (a) Schematic structure of P(VDF-TrFE-CFE) in relaxed and ferroelectric state. (b) Dielectric constant of P(VDF-TrFE-CFE) at temperatures between 200 and 340 K at the frequencies of 0.3 kHz, 3 kHz, 30 kHz, and 300 kHz. P(VDF-TrFE-CFE) transfers from relaxor to ferroelectric when the temperature is below T_c. (c) The ferroelectric hysteresis loops of 200 nm P(VDF-TrFE-CFE) film capacitor at different temperatures. It is measured using Sawyer–Tower circuit at a frequency of 1 Hz. (d) Transfer characteristic curves of the bilayer WSe_2 channel with a P(VDF-TrFE-CFE) ferroelectric polymer top gate and SiO_2 back gate at room temperature. The field effect mobility as a function of V_g is shown in the inset.

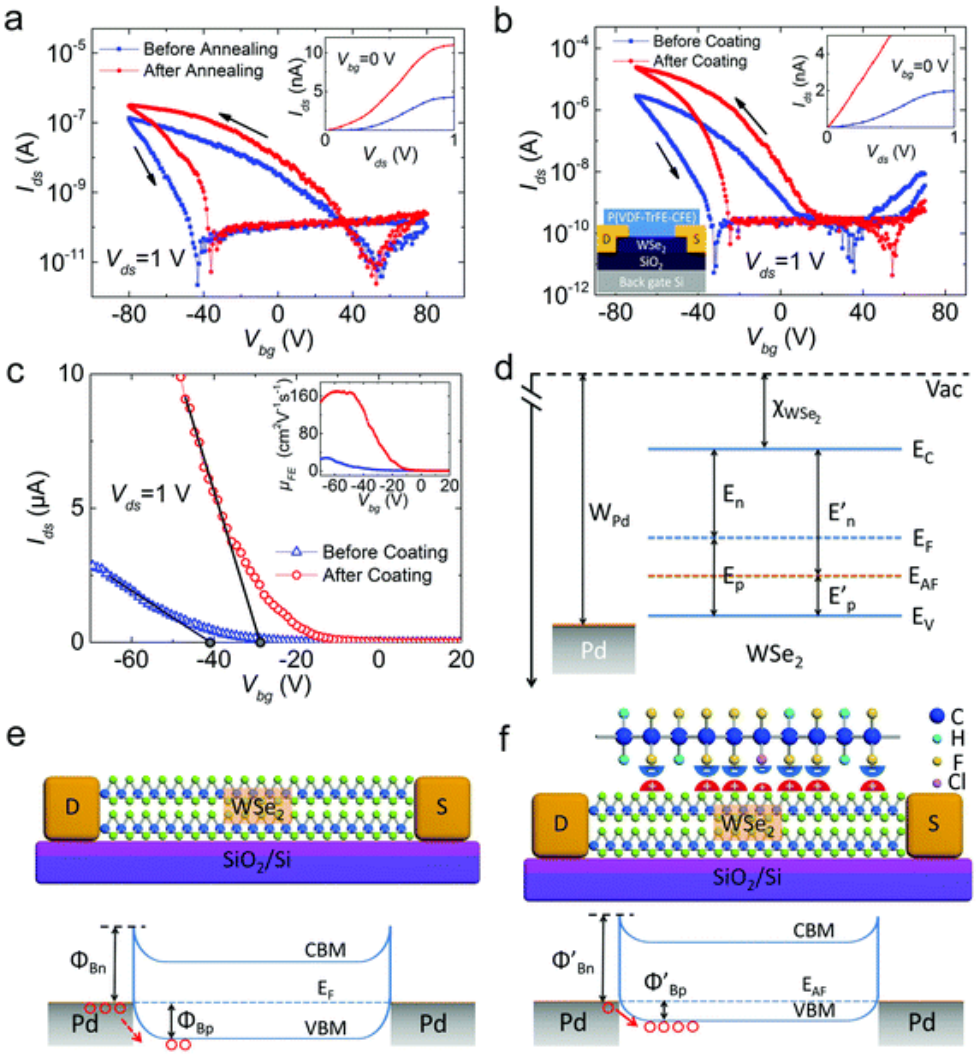


Fig. 3 Electrical properties of few layers WSe_2 FETs treated by annealing and p-doping. (a) Transfer and output curves (inset) of a bilayer WSe_2 FET before and after annealing at 200 °C under an argon atmosphere for 2 hours. (b) Transfer and output curves (right inset) of a six-layered WSe_2 FET before and after coating with P(VDF-TrFE-CFE). The cross-section structure of the device after coating is shown in the left inset. (c) Transfer curves in linear coordinate from 20 V to −70 V of the six-layered WSe_2 FET before and after coating with P(VDF-TrFE-CFE). The field effect mobility as a function of V_{bg} is shown in the inset. (d) Schematic of the band structure between WSe_2 and Pd contact metal, and E_F and E_{AF} are the Fermi level before and after coating with P(VDF-TrFE-CFE), respectively. (e and f) Schematic structure and energy band diagrams of WSe_2 FET gated by SiO_2 before and after coating with P(VDF-TrFE-CFE), respectively.

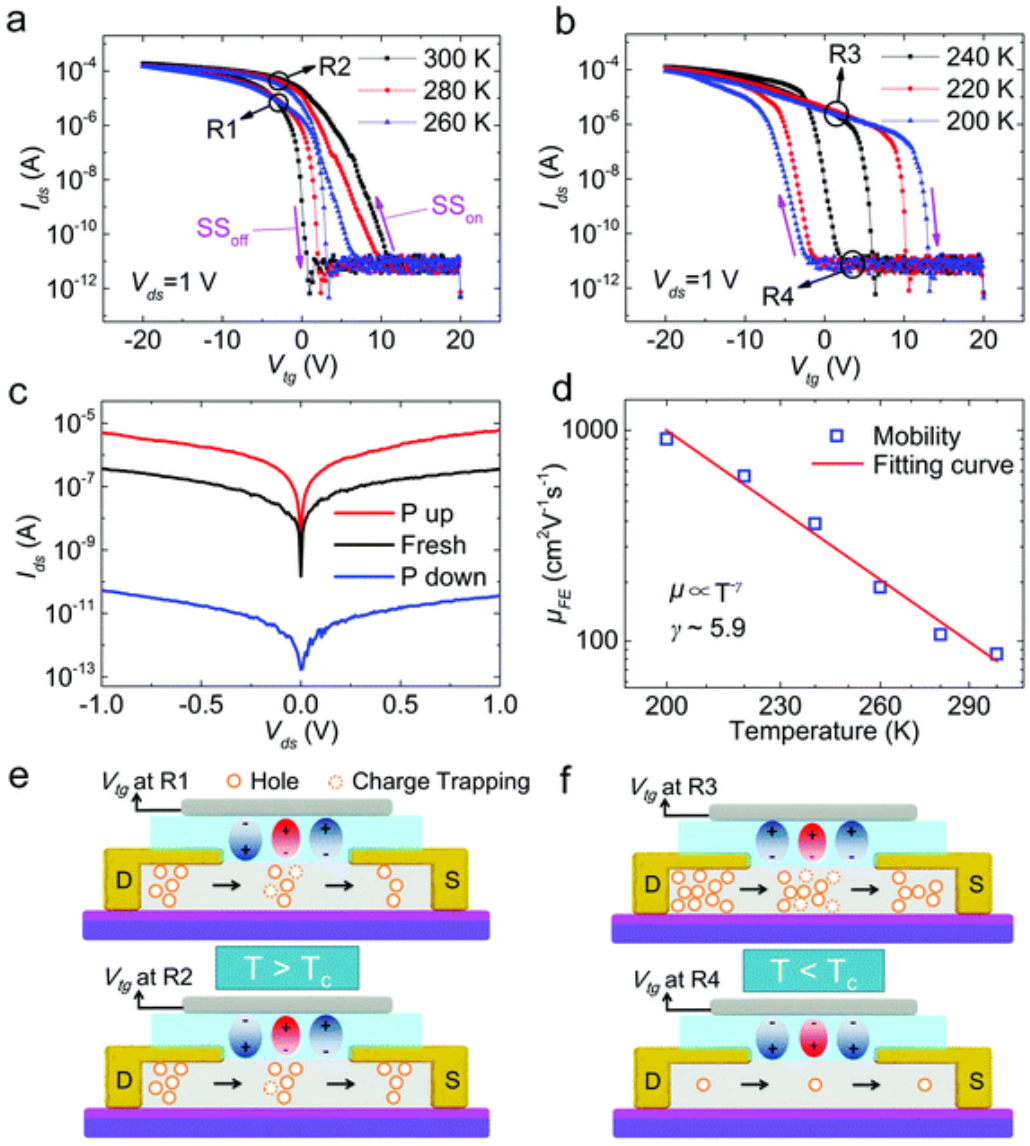


Fig. 4 Ferroelectricity-related electrical properties of the device. (a) Transfer characteristic curves at temperatures beyond T_c. (b) The transfer characteristic curves at temperatures below T_c. (c) Output characteristic curves without an external gate voltage in three states of ferroelectric layer at 200 K. The three states are fresh state (ferroelectric layer without polarization), *P* up state (polarized by $V_{tg} = -20$ V), and *P* down state (polarized by $V_{tg} = 20$ V). (d) Experimental and fitted date of temperature dependence of field effect hole mobility μ_{FE}. (e) Schematic of the influence of the transition process of P(VDF-TrFE-CFE) on the charge trapping at $T > T_c$ and V_{tg} in region R1 and R2 in (a), and (f) at $T < T_c$ and V_{tg} in region R3 and R4 in (b).

Table 1 Comparison of electrical performance of WSe_2-based FETs at room temperature

Treatment	Dielectric	ON current (A)	ON/OFF ratios	Field effect hole mobility ($cm^2\ V^{-1}\ s^{-1}$)	V_{th} (V)	Ref.
P(VDF-TrFE-CFE) doping	SiO_2	4×10^{-5}	3×10^5	170.9	On: −29 Off: −50	This work
	P(VDF-TrFE-CFE)	2×10^{-4}	2×10^7	86.7	On: +2 Off: −1.2	This work
MoO_3 doping	SiO_2	$\sim 10^{-5}$	$\sim 10^5$	98.7	—	25
NO_2 chemical doping	ZrO_2	$\sim 10^{-5}$	$\sim 10^6$	~250	—	28
Gold deposition	Ion Gel	$\sim 10^{-3}$	$\sim 10^6$	96.6	+0.95	30
OTS doping	SiO_2	$\sim 10^{-5}$	$\sim 10^7$	105–192	−0.45	31

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