WILEY-VCH

DOI: 10.1002/((please add manuscript number))
Article type: Communication

Low-Voltage, Optoelectronic $CH_3NH_3PbI_{3-x}Cl_x$ Memory with Integrated Sensing and Logic Operations

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Keywords: perovskite, resistive switching memory, optoelectronic memory, logic operation, coincidence detection

Abstract- Non-volatile optoelectronic memories integrated with the functions of sensing, data storage and data processing are promising for the potential Internet of Things (IoT) application. To meet the requirements of IoT devices, multifunctional memory devices with low power consumption and secure data storage are highly desirable. Here we demonstrate an optoelectronic resistive switching memory integrated with sensing and logic operations by adopting organic-inorganic hybrid $CH_3NH_3PbI_{3-x}Cl_x$ perovskites, which possess unusual defect physics and excellent light absorption. The $CH_3NH_3PbI_{3-x}Cl_x$ cell exhibits low operation voltage of 0.1 V with the assistance of light illumination, long-term retention property, and multiple resistance states. Its unique optoelectronic characteristics enable to perform logic operation for inputting one electrical pulse and one optical signal, and detect the coincidence of electrical and optical signal as well. This design provides possibilities for smart sensor in IoT application.

Internet of things (IoT) has emerged as a technological revolution in the information explosion era. There are huge amount of interconnected devices coupled with sensors (data capture), processors (data processing and analyzing), and embedded non-volatile memories (data storage). To better deliver the potential of IoT, multifunctional integrated devices with low power consumption are desired. From this point of view, non-volatile optoelectronic memory can be a possible choice for constructing a "smart sensor" for IoT application, which integrates the sensing, data storage and data processing functions into one device.

Optoelectronic memory can respond to both electrical stimuli and optical excitation, which enables to store and convert optical information as an electronic readout at low programming voltages.[1-5] The optoelectronic memory also takes advantages of storing and processing transmitted optical signals over long-distance transmission with wide bandwidth, high-data-rate density, and low power consumption. [6] Recently, researchers have demonstrated optoelectronic memory devices integrated with multi-level data storage, light-sensing, demodulating and arithmetic functions. [1, 4, 5, 7-9] However, new optoelectronic materials, architectures and systems still remain to be developed and explored to reduce the cost, complexity and energy consumption.

Recently, organometal halide perovskites (OHPs) show excellent light absorption, long electron-hole diffusion length, ambipolar charge transport, unusual defect physics, and tunable band gap. [10] A number of applications based on OHPs as light absorbing materials or semiconductor materials have been demonstrated, including solar cell [11-13], photodetector[14, 15], laser[16], light emitting diode [17-20], transistors[21] and photovoltachormic supercapacitor[22]. OHP-based electronic devices usually exhibit significant hysteresis, possibly caused by ferroelectricity, the formation and movement of trap states or ion migration in the perovskites. More recently, researchers reported the perovskites for non-volatile resistive switching random access memory

(RRAM).[23-27] Till now, most of the research works based on the perovskite memory have been focused on the tri-iodide perovskite ($CH_3NH_3PbI_3$) system. It has been verified that I^- and MA^+ with low activation energies can migrate under external electric field.[28] The formation and accumulation of defects can lead to resistive switching (RS) behavior in the perovskite memory devices.[23, 27] It is also desirable to develop device architecture or counterpart materials, which enable the integration of both non-volatile information storage and processing in one device for the sake of high-performance integrated circuit design.

In this work, we design a non-volatile optoelectronic $CH_3NH_3PbI_{3-x}Cl_x$ memory device, in which the SET voltage can be controlled as low as 0.1 V with the assistance of light illumination. The $CH_3NH_3PbI_{3-x}Cl_x$ memory device can execute data-storage and logic operation in one memory device by using one electrical pulse and one optical pulse as the input signals. It can also detect the coincidence of electric and optical signal. This design provides possibilities in smart sensor design and IoT application.

Figure 1a shows schematic structure of perovskite based memory in a configuration of Au/$CH_3NH_3PbI_{3-x}Cl_x$ hybrid perovskite/fluorine-doped tin oxide (FTO) substrate, where the bottom FTO electrode is grounded, and the top Au electrode is connected to a voltage source for switching the memory cell. The perovskite thin film ($CH_3NH_3PbI_{3-x}Cl_x$) was deposited on FTO glass substrate by one-step solution method, and 50 nm Au was deposited on top of perovskite layer by e-beam evaporation. Figure 1b is the top-view scanning electron microscopy (SEM) image of the perovskite layer with a thickness of 270 nm, indicating a continuous perovskite film and good coverage on the FTO substrate. The (110), (220) and (330) peaks in the X-Ray diffraction (XRD) patterns confirms a crystallized perovskite thin film with the tetragonal phase, as shown in Figure 1c. To determine the elemental composition in the perovskite layer, we also conducted X-

ray photoelectron spectroscopy (XPS) test (Figure 1d). A full spectrum scan shows negligible amount of Cl atoms in the perovskite film. A narrow scan of Cl 2p core level is shown in the Figure S1, where negligible signals corresponding to the Cl $2p_{3/2}$ and Cl $2p_{1/2}$ peaks are detected. It is consistent with previous works, in which the presence of Cl involves in the form of intermediate phase CH_3NH_3Cl that can easily escape during the annealing process and rare Cl exists in the final product.[29] Although Cl content is negligible in the final perovskite thin film, Cl plays an important role in the film formation and crystallization and can influence the surface trap states in the film and the electronic properties [29-31].

It is worthy to be noted that we intentionally introduced the traps in the $CH_3NH_3PbI_{3-x}Cl_x$ film for the resistive switching memory device by using a low-concentrated precursor solution (34 wt. %). It has been suggested that the role of Cl in the precursor solution (>45 wt. %) can slow down the perovskite formation and crystallization, and drive the growth of well-defined grains in the perovskite film because of the modulated kinetics of the reactions by the formation of intermediate phases (*e.g.* CH_3NH_3Cl).[29, 30] This evolution in perovskite morphology can further results in the reduced trap states and long diffusion length in the perovskite film.[32-34] However, due to the less content of CH_3NH_3Cl in the low-concentrated precursor solution, the duration of CH_3NH_3Cl controlled crystallization is shortened and results in the under-developed film.[29] This can introduce increased trap states during the film formation, and is a dominant characteristic in understanding the switching mechanism of our memory device.

We first examine the electrical characteristics of $CH_3NH_3PbI_{3-x}Cl_x$ based RRAM. **Figure 2** shows the characteristics of electrical switching of $CH_3NH_3PbI_{3-x}Cl_x$ based memory. The memory device exhibits a bipolar and non-volatile resistive switching behavior (Figure 2a) under a DC voltage bias sweep (0 →1.5→0→-1.5 →0 V). No forming process is required. As a positive

voltage sweep is applied from 0 V to 1.5 V, the device is triggered from high resistance state (HRS) to low resistance state (LRS) at a positive voltage of 1.47 V. The RESET process occurs by applying a negative voltage of -1.41 V. The ON/OFF ratio of the perovskite memory cell reaches 10^4. Figure 2b and 2c demonstrate the retention characteristic and cyclic endurance test during 50 cycles, respectively. All of the above electrical tests are performed under a dark condition. Distributions of the average SET/RESET voltage of the devices in 17 batches are shown in Figure 2d. The devices fabricated in different batches exhibit reasonable variations with similar performance.

The unique light absorption characteristics of perovskite provide the possibilities in controlling the switching behavior and realizing more functions in $CH_3NH_3PbI_{3-x}Cl_x$ memory. **Figure** 3a depicts the current-voltage (I-V) characteristics of the photo-assisted switching. During the SET process, the white light LED with a power density of 3.20 mW/cm^2 is adopted to illuminate the device from the FTO side, accompanying with the positive voltage sweep. It is noteworthy that the transition from HRS to LRS occurs at a SET voltage as low as 0.1 V, which is the lowest SET voltage compared with those perovskite based RRAM cells reported in existing literature. In these previous works, the SET voltages of perovskite based non-volatile RRAM under dark condition are 0.64 V [23], 0.8 V [24] and 2 V [28], respectively. After the SET process, the device can be electrically RESET under a dark condition at a voltage of -0.45 V. Distributions of the average SET/RESET voltage and HRS/LRS are plotted in Figure 3b and Figure S4, respectively, showing reasonably good memory characteristics. We also conducted endurance and retention measurements using pulse measurement mode, as shown in Figure 3c and 3d. The voltage pulse condition and light power density for SET process is 0.13 V for 100 μs and 3.2 mW/cm^2, respectively. The voltage pulse for RESET process is −1.6 V for 250 μs. The readout voltage is

0.05 V. Figure 3c depicts pulse switching endurance for two resistance states over 400 cycles. Both HRS and LRS can be retained up to 13 hours under dark and ambient environment, showing good retention compared with other perovskite-based memories (Figure 3d).[23-28] The switching performance of our device is in stark contrast with the existing optoelectronic memories. In the previous optoelectronic memories reported, the memory devices can perform well through optical switching with light illumination. While there is no optical power supplied and under a dark condition, the electrical switching cannot exhibit comparable performances. For example, the optoelectronic memory with ITO/CeO_{2-x} /Al_xO_y/Al structure can be switched optically with an ON/OFF ratio of 10^3, whereas only an ON/OFF ratio of 10 is exhibited in the electrical switching under dark condition because of a different switching mechanism. [8] Similar phenomena have also been demonstrated in optoelectronic memories based on other materials, such as ZnO/$SrTiO_3$ [8] and Al_2O_3/SiO_2/Si [3]. In comparison, our device can exhibit similar ON/OFF ratio by electrical switching under the dark condition compared with the switching under light illumination, which can be more adaptive to various environments.

Figure 3e and 3f present the photo-assisted switching characteristics. The SET voltage exhibits light-dependent characteristics, as shown in the Figure 3e. As the light intensity is increased from 0 to 3.20 mW/cm^2, the SET voltage decreases from 1.47 V to 0.1 V accordingly with the same compliance current of 10 mA. By combining voltage pulse and optical pulse, we can also obtain multiple non-volatile resistance states corresponding to different light intensities (Figure 3f). The SET processes of each resistance state are operated by one electrical pulse and one optical pulse. The voltage pulse used is 0.13 V 100 μs for all set processes. The duration of optical pulse applied is 1 s and the readout voltage is 0.05 V. With the same voltage pulse, the resistance of memory cell is decreased as light intensity is increased. These light intensity-dependent characteristics can

also be considered as behaviors of a sensor, in which the resistance switching behaves differently according to different levls of light intensities. Compared with the conventional photodetector, the light information can be recorded and retained in our device even after the removal of optical trigger.

In order to better understanding the switching behavior and switching mechanism, firstly we conducted the ultraviolet electron microscopy (UPS) to examine the surface trap states and semiconductor type of the as-prepared perovskite thin film on the FTO glass, which plays an important role in determining the electronic properties of the perovskite film. [35, 36] A He-I UV light source ($h\nu$=21.2 eV) is utilized to obtained the UPS spectra (Figure 1e and 1f). The binding energy is referred to the Fermi level. We extract the work function from the onset energy in the cut-off region in Figure 4a, which is approximately 4.37 eV. Figure 4b shows the spectrum near the valence band region, where the valence band maxima (VBM) is obtained at a binding energy of 1.32 eV. The band gap of perovskite thin film is determined to be 1.63 eV, according to the absorption spectrum in Figure S2. Thus, the schematic band diagram of perovskite thin film can be sketched in the inset of Figure 4b, in which the Fermi level locates near to the conduction band. In addition, UPS has a high sensitivity to the intrinsic surface defects. A broad distribution of hole trap states is presented in the band gap above the valence energy. In previous studies, researchers also employed UPS technique to examine the surface trap states in the perovskite thin film, which are in consistent with our results [37, 38] These trap states can provide hole trapping centers at the perovskite/Au interface, which is essential to understand the switching behavior in the $CH_3NH_3PbI_{3-x}Cl_x$ memory device.

Secondly, we investigated the effect of device area on the resistance state. Figure 4c (electrical switching) and Figure 4d (photo-assisted switching) show the ON and OFF current of our

perovskite memory devices with different device areas (the diameter of top electrode: 80 μm, 150 μm, and 300 μm). The readout voltage is 0.05 V and compliance current is controlled at 10 mA. The resistance increases with the decrease of device area. This is in stark contrast with the filament-based switching mechanism, where the resistance is typically independent on device area. According to the above area-dependent results and UPS tests, we proposed an interface-based switching mechanism based on the injection/ejection of holes at the perovskite/Au interfacial hole trapping centers.

Figure 4e depicts the proposed mechanisms of electrical switching of the perovskite memory cell. According to the UPS characterization results, the work function of perovskite is 4.37 eV and the interfacial hole traps are located close to valence bands. At the initial state (HRS), there is a Schottky barrier formed at the perovskite/Au interface because of the difference in Fermi level between perovskite (4.37 eV) and Au (5.0 eV). The work function of the FTO glass is extracted as 4.33 eV from the UPS, as shown in Figure S4. Thus, we can regard the contact between FTO and perovskite as Ohmic contact because of their similar work functions of 4.33 eV (FTO) and 4.37 eV ($CH_3NH_3PbI_{3-x}Cl_x$), respectively.

As a positive voltage connected to Au electrode is increased to 1.5 V, the Schottky barrier is decreased. The holes can inject from the Au electrode across the perovskite/Au interface, and fill into the interfacial hole trapping centers. With the increase of hole concentration at the interface, the Fermi level of perovskite shift towards to the valence band, leading to a lowered Schottky barrier. The contact between perovskite and Au electrode then becomes a quasi Ohmic contact, corresponding to LRS. Hybrid perovskite has been reported previously that can be heavily doped in low concentration dopants, which results in the obvious change in Fermi level and Schottky barrier.[39-41] Since the hole trap states have broad energy distribution between the Fermi level and

valence band maximum (Figure 4b), the injected holes can be stably filled in the deep level defects, and the LRS can be retained even after the removal of electrical bias.[42-45] The RESET process happens as a negative voltage bias is applied to the Au electrode. Holes are retracted from the trapped states in perovskite to the Au electrode. The Schottky barrier becomes higher and recovers to the original state (HRS).

For the photo-assisted low voltage switching (Figure 4f), under the light illumination, a large amount of electron-hole pairs are generated in the perovskite that can be separated with a small bias of 0.1 V. The hole trap states can trap photo-generated holes, shifting the Fermi level of perovskite towards valence band and leaving a lowered Schottky barrier. In the meantime, more holes from Au electrode can also inject into the hole trap states in the perovskite, further lowering the Schottky barrier. A quasi Ohmic contact can be formed, corresponding to LRS. Thus, with the light illumination, the SET voltage of the device can be controlled as low as 0.1 V, and the energy consumption of the memory device can also be reduced in this photo-assisted switching. The SET voltage also exhibits the light-intensity dependent characteristics. As the light intensity decreases, less amount of photo-induced charge carriers are generated, which requires a larger voltage to drive the injection of holes. By combining voltage pulse and optical pulse, multiple resistance states can be obtained. With the same voltage pulse (0.13 V, 100 μs) and higher light intensity, the number of filled hole traps is increased, resulting in decreased Schottky barrier and resistance.The RESET process is similar to that of the electrical switching as stated above.

In addition to the sensing and memory functions, the use of both optical and electrical pulses also enables the device to operate with the functions of both data storage and non-volatile logic operation. Here we adopt the light pulses and electrical pulses as the input signals to realize typically logic operation, including AND (Y=AB) and OR (Y=A+B). **Figure 5**a demonstrates a

nonvolatile AND logic operation. To correctly perform a logic operation, it is critical to select the light intensity and pulse voltage. For the input signals, we defined the light pulse (>3.2 mW/cm^2, 1 s) as logic '1', light pulse (<0.3 mW/cm^2, 1 s) as logic '0', electrical pulse (0.13 V, 100 μs) as logic '1' and electrical pulse (0.01 V, 100 μs) as logic '0'. For the output, the HRS and LRS are defined as logic '1' and logic '0', respectively. The output currents are read before and after the input pulses with a read voltage of 0.05 V. Using an electrical pulse with a small voltage of 0.01 V, even combining a light pulse with intensity of >3.2 mW/cm^2, the memory device cannot be switched to LRS. This can be understood that the voltage of 0.01 V is insufficient to separate the photo-generated carriers or drive the charge carriers into hole traps. Similarly, the use of a light pulse with low power intensity of <0.3 mW/cm^2 and an electrical pulse of 0.1 V is not enough to set the device to LRS, because of the very small amount of photo-generated charge carriers produced. Only in the case that the input electrical pulse (0.1 V, 1 s) and optical pulse (3.2 mW/cm^2, 1 s) can switch the device to LRS corresponding to logic '1'. The output state of LRS can be retained over 13 hours.

To fulfill an OR logic operation, we also appropriately select the parameters of the input pulses. Figure 5b show an OR logic operation. Before each operation, the device is reset to HRS. In the OR logic operation, we define the light pulse (3.2 mW/cm^2, 1 s) as logic '1', light pulse (0.5 mW/cm^2, 1 s) as logic '0', electrical pulse (2 V, 250 μs) as logic '1' and electrical pulse (0. 13 V, 100 μs) as logic '0'. The output currents are read before and after the input pulses with a read voltage of 0.05 V. As an electrical pulse of 0.13 V and an optical pulse of 0.5 mW/cm^2 are input, the input energy cannot drive the SET process, and the output is considered as logic '0'. The inputs of an electrical pulse of 0.1 V (logic "0") and a light pulse of 3.2 mW/cm^2 (logic "1"), and inputs of an electrical pulse of 2 V (logic "1") and a light pulse of 0.5 mW/cm^2 (logic "0") can both switch

the device to LRS (logic "1"). The output states can be stably retained and stored, which suggests a non-volatile logic operation.

We also demonstrate another function of coincidence event detection in our device, which can detect the simultaneity the several input signals and plays important roles in the neuroscience and neuromorphic computing. [46-48] Figure 5c shows the operation of the perovskite memory as a 3-pulse coincidence detector. In this system, three input signals are defined as optical pulse (A) with a power intensity of 3.2 mW/cm^2, electrical pulse (B) applied to the top electrode (0.05 V) and electrical pulse (C) applied to the bottom electrode (-0.05 V). The duration of three pulses are 1 s. The output current Y can represent if one of the input signal is out of phase with the rest signals. It can be noticed that only in the case the three pulses appear simultaneously, there shows the output current of 1.4 mA, corresponding to the LRS of the memory device.

In summary, we design and fabricate $CH_3NH_3PbI_{3-x}Cl_x$ perovskite based optoelectronic memory device. By utilizing the excellent light absorption ability of the perovskite layer, the SET voltage of the memory device can be decreased from 1.5 V to 0.1 V with the assistance of light illumination. It can reduce the power consumption in the device. According to the switching behavior, we proposed a possible trap-mediated switching mechanism based on the existence of hole trapping centers at the $CH_3NH_3PbI_{3-x}Cl_x$ perovskite surface. The possible switching mechanism may provide more possibilities in the perovskite based memory device design. By combining the electrical input and optical input and correctly select the input pulses, the perovskite RRAM can execute not only data storage but also optical sensing and logic operation.

Experimental Section

*Perovskite Deposition and Perovskite Based ReRAM Fabrication***:** The fluorine-doped tin oxide (FTO) coated glass substrates were cleaned with acetone, isopropanol and deionized water sequentially. The pre-cleaned substrates were then dried with nitrogen gas and further cleaned by UV-Ozone treatment. A one-step spin coating was applied to the deposition of perovskite layer ($CH_3NH_3PbI_{3-x}Cl_x$) on the FTO glass in the N_2 glove box. The spin coating solution (34-wt%) for the perovskite layer was prepared by mixing methylammonium iodied (MAI) and lead chloride in N, N-dimethylformamide (DMF). The spin-coated perovskite thin film was annealed at 105 ºC for 40 min. The dot-shaped Au electrodes with a thickness of 50 nm and diameter of 200 μm were deposited by e-beam evaporation through a shadow mask. The deposition rate was controlled at 0.3 Å /s and the final deposition temperature of the substrate was 40 °C.

Characterization of Perovskite Thin Film: X-Ray diffraction (XRD) patterns of the perovskite film was determined by a Rigaku SmartLab X-ray diffractometer with a 2 theta range from 10 º to 70 º in a step of 0.01 º. Scanning electrom microscopy (SEM) image was performed by Hitachi S-4800 field emission scanning microscope. The absorption spectra of perovskite film on quartz were examined using a UV-2250 Shimadzu UV-Vis spectrophotometer. Ultraviolet photoelectron spectra (UPS) and X-ray photoelectron spectroscopy (XPS) were carried out in a vacuum chamber ($<10^{-5}$ Torr). The excitation source for UPS is He-I UV source (hν =21.2 eV). Before the UPS measurement of the perovskite sample, a conductive Au sample is used to calibrate the Fermi level. As to conduct the UPS of perovskite layer, a small voltage bias 5 V is applied to the sample when recording the secondary electron cutoff. A monochromatic Al Ka (1486.6 eV photons) was used as the excitation source for XPS. A pass energy of 80 or 40 eV was employed for the wide and core-level narrow scan, respectively. The core-level signals were recorded at a photoelectron take-off angle of 90°. All binding energies were calibrated referring to the C1s peak at 284.6 eV.

Characterization of Perovskite Based ReRAM: The electrical characterizations of perovskite based ReRAM were measured using a Keithley 4200 in the vacuum probe station. FTO electrode was grounded and voltage was applied to the gold electrode. A white light LED with controllable power densities was used to illuminate the device from the FTO side. All the electrical switching measurements were conducted in the dark.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported by the Research Grant Council of Hong Kong (grant No.: PolyU 252001/14E) and the Hong Kong Polytechnic University (grant No: 1-ZE25, 1-ZVK1 and 1-ZVGH).

Received: ((will be filled in by the editorial staff))

Revised: ((will be filled in by the editorial staff))

Published online: ((will be filled in by the editorial staff))

[1] A. Lipatov, P. Sharma, A. Gruverman, A. Sinitskii, *ACS nano* **2015**, *9*, 8089.
[2] A. Bera, H. Peng, J. Lourembam, Y. Shen, X. W. Sun, T. Wu, *Adv. Funct. Mater*. **2013**, *23*, 4977.
[3] M. Ungureanu, R. Zazpe, F. Golmar, P. Stoliar, R. Llopis, F. Casanova, L. E. Hueso, *Adv. Mater*. **2012**, *24*, 2496.
[4] J. Lee, S. Pak, Y.-W. Lee, Y. Cho, J. Hong, P. Giraud, H. S. Shin, S. M. Morris, J. I. Sohn, S. Cha, *Nat. Commun*. **2017**, *8*, 14734.
[5] K. Roy, M. Padmanabhan, S. Goswami, T. P. Sai, G. Ramalingam, S. Raghavan, A. Ghosh, *Nat. Nanotech*. **2013**, *8*, 826.
[6] M. J. Kobrinsky, B. A. Block, J.-F. Zheng, B. C. Barnett, E. Mohammed, M. Reshotko, F. Robertson, S. List, I. Young, K. Cadien, *Intel Technology Journal* **2004**, *8*.
[7] M. S. Choi, G.-H. Lee, Y.-J. Yu, D.-Y. Lee, S. H. Lee, P. Kim, J. Hone, W. J. Yoo, Nat. Commun. **2013**, *4*, 1624.

[8] H. Tan, G. Liu, X. Zhu, H. Yang, B. Chen, X. Chen, J. Shang, W. D. Lu, Y. Wu, R. W. Li, Adv. Mater. **2015**, *27*, 2797.
[9] C.-J. Kim, S.-J. Choi, J.-H. Ahn, J.-W. Han, H. Kim, S. Yoo, Y.-K. Choi, ACS nano **2012**, *6*, 1449.
[10] S. D. Stranks, G. E. Eperon, G. Grancini, C. Menelaou, M. J. Alcocer, T. Leijtens, L. M. Herz, A. Petrozza, H. J. Snaith, Science **2013**, *342*, 341.
[11] J. Burschka, N. Pellet, S.-J. Moon, R. Humphry-Baker, P. Gao, M. K. Nazeeruddin, M. Grätzel, *Nature* **2013**, *499*, 316.
[12] J. M. Ball, M. M. Lee, A. Hey, H. J. Snaith, *Energy Environ. Sci*. **2013**, *6*, 1739.
[13] M. Long, T. Zhang, H. Zhu, G. Li, F. Wang, W. Guo, Y. Chai, W. Chen, Q. Li, K. S. Wong, *Nano Energy* **2017**, *33*, 485.
[14] W. Deng, L. Huang, X. Xu, X. Zhang, X. Jin, S.-T. Lee, J. Jie, *Nano Lett* **2017**, *17*, 2482.
[15] L. Dou, Y. M. Yang, J. You, Z. Hong, W.-H. Chang, G. Li, Y. Yang, *Nat. Commun*. **2014**, *5*, 5404.
[16] H. Zhu, Y. Fu, F. Meng, X. Wu, Z. Gong, Q. Ding, M. V. Gustafsson, M. T. Trinh, S. Jin, X. Zhu, *Nat. Mater*. **2015**, *14*, 636.
[17] Y. H. Kim, H. Cho, J. H. Heo, T. S. Kim, N. Myoung, C. L. Lee, S. H. Im, T. W. Lee, *Adv. Mater.* **2015**, *27*, 1248.
[18] S. A. Veldhuis, P. P. Boix, N. Yantara, M. Li, T. C. Sum, N. Mathews, S. G. Mhaisalkar, *Adv. Mater.* **2016**, *28*, 6804.
[19] H. Cho, C. Wolf, J. S. Kim, H. J. Yun, J. S. Bae, H. Kim, J. M. Heo, S. Ahn, T. W. Lee, *Adv. Mater*. **2017**, *29*, 31.
[20] H. K. Seo, H. Kim, J. Lee, M. H. Park, S. H. Jeong, Y. H. Kim, S. J. Kwon, T. H. Han, S. Yoo, T. W. Lee, *Adv. Mater*. **2017**, *29*, 12.
[21] M. Long, T. Zhang, Y. Chai, C.-F. Ng, T. C. Mak, J. Xu, K. Yan, *Nat. Commun*. **2016**, *7*, 13503.
[22] F. Zhou, Z. Ren, Y. Zhao, X. Shen, A. Wang, Y. Y. Li, C. Surya, Y. Chai, *ACS nano* **2016**, 10, 5900.
[23] C. Gu, J.-S. Lee, ACS nano **2016**, *10*, 5413.
[24] E. J. Yoo, M. Lyu, J. H. Yun, C. J. Kang, Y. J. Choi, L. Wang, *Adv. Mater.* **2015**, *27*, 6170.
[25] Z. Xiao, J. Huang, *Adv. Electron. Mater*. **2016**, *2*,7.
[26] W. Xu, H. Cho, Y. H. Kim, Y. T. Kim, C. Wolf, C. G. Park, T. W. Lee, *Adv. Mater*. **2016**, *28*, 5916.
[27] D. J. Kim, Y. J. Tak, W. G. Kim, J. K. Kim, J. H. Kim, H. J. Kim, *Adv. Mater. Interfaces* **2017**, *4*, 6.
[28] X. Zhu, J. Lee, W. D. Lu, *Adv. Mater*. **2017**, *29*, 29.
[29] H. Yu, F. Wang, F. Xie, W. Li, J. Chen, N. Zhao, *Adv. Funct. Mater*. **2014**, *24*, 7102.
[30] Q. Chen, H. Zhou, Y. Fang, A. Z. Stieg, T.-B. Song, H.-H. Wang, X. Xu, Y. Liu, S. Lu, J. You, *Nat. Commun*. **2015**, *6,*7269.
[31] S. Colella, E. Mosconi, P. Fedeli, A. Listorti, F. Gazza, F. Orlandi, P. Ferro, T. Besagni, A. Rizzo, G. Calestani, *Chem. Mater*. **2013**, *25*, 4613.
[32] F. X. Xie, H. Su, J. Mao, K. S. Wong, W. C. Choy, *J. Phys. Chem.* C **2016**, *120*, 21248.
[33] R. J. Stewart, C. Grieco, A. V. Larsen, G. S. Doucette, J. B. Asbury, *J. Phys. Chem.* C **2016**, *120*, 12392.
[34] E. M. Hutter, G. E. Eperon, S. D. Stranks, T. J. Savenije, *J. Phys. Chem. Lett* **2015**, *6*, 3082.

[35] K. Jiao, C. Duan, X. Wu, J. Chen, Y. Wang, Y. Chen, *Phys. Chem. Chem. Phys*. **2015**, *17*, 8182.
[36] A. Pfau, K. Schierbaum, *Surf. Sci*. **1994**, *321*, 71.
[37] X. Wu, M. T. Trinh, D. Niesner, H. Zhu, Z. Norman, J. S. Owen, O. Yaffe, B. J. Kudisch, X.-Y. Zhu, *J. Am. Chem. Soc*. **2015**, *137*, 2089.
[38] Y.-F. Chen, Y.-T. Tsai, D. Bassani, R. Clerc, D. Forgács, H. Bolink, M. Wussler, W. Jaegermann, G. Wantz, L. Hirsch, *J. Mater. Chem. A* **2016**, *4*, 17529.
[39] J. M. Frost, K. T. Butler, F. Brivio, C. H. Hendon, M. Van Schilfgaarde, A. Walsh, *Nano Lett*. **2014**, *14*, 2584.
[40] K. Yan, M. Long, T. Zhang, Z. Wei, H. Chen, S. Yang, J. Xu, *J. Am. Chem. Soc*. **2015**, *137*, 4460.
[41] K. Yan, Z. Wei, T. Zhang, X. Zheng, M. Long, Z. Chen, W. Xie, T. Zhang, Y. Zhao, J. Xu, *Adv. Funct. Mater*. **2016**, *26*, 8545.
[42] G. Agnus, W. Zhao, V. Derycke, A. Filoramo, Y. Lhuillier, S. Lenfant, D. Vuillaume, C. Gamrat, J. P. Bourgoin, *Adv. Mater*. **2010**, *22*, 702.
[43] K. Das, M. NandaGoswami, R. Mahapatra, G. Kar, A. Dhar, H. Acharya, S. Maikap, J.-H. Lee, S. Ray, *Appl. Phys. Lett*. **2004**, *84*, 1386.
[44] C.-H. Lin, Y. Kuo, *J. Appl. Phys.* **2011**, *110*, 024101.
[45] M. V. Srinivasan, G. D. Bernard, *Biol. Cybern*. **1976**, *21*, 227.
[46] K. D. Cantley, A. Subramaniam, H. J. Stiegler, R. A. Chapman, E. M. Vogel, *IEEE Trans. Neural Netw. Learn. Syst*. **2012**, *23*, 565.
[47] P. König, A. K. Engel, W. Singer, *Trends Neurosci.* **1996**, *19*, 130.
[48] H. Agmon-Snir, C. E. Carr, J. Rinzel, *Nature* **1998**, *393*, 268.

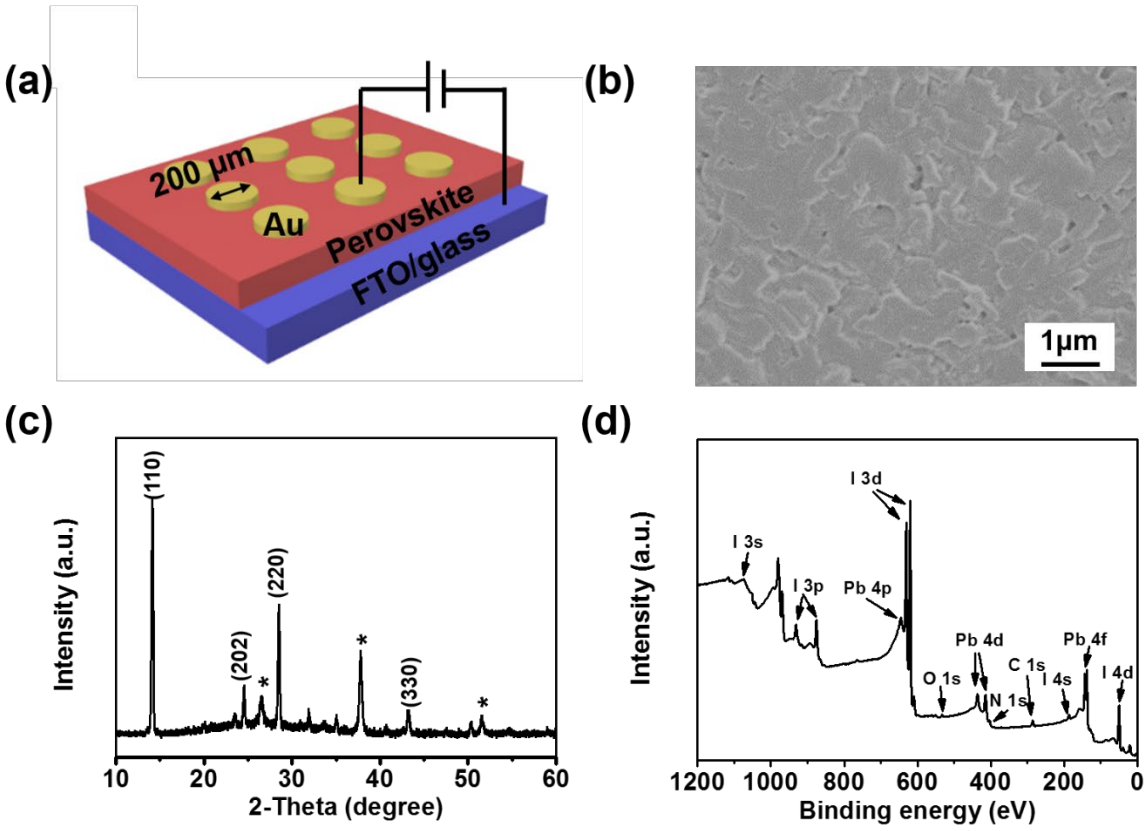

Figure 1. (a) Schematic device structure of perovskite based RRAM. (b) The as-prepared perovskite thin film deposited on FTO glass substrate by one-step solution method, indicating good coverage of perovskite layer on the FTO glass. (c) XRD patterns of the as-prepared perovskite thin film. * represents the peaks of FTO glass. (d) XPS survey spectrum of the as-prepared perovskite thin film.

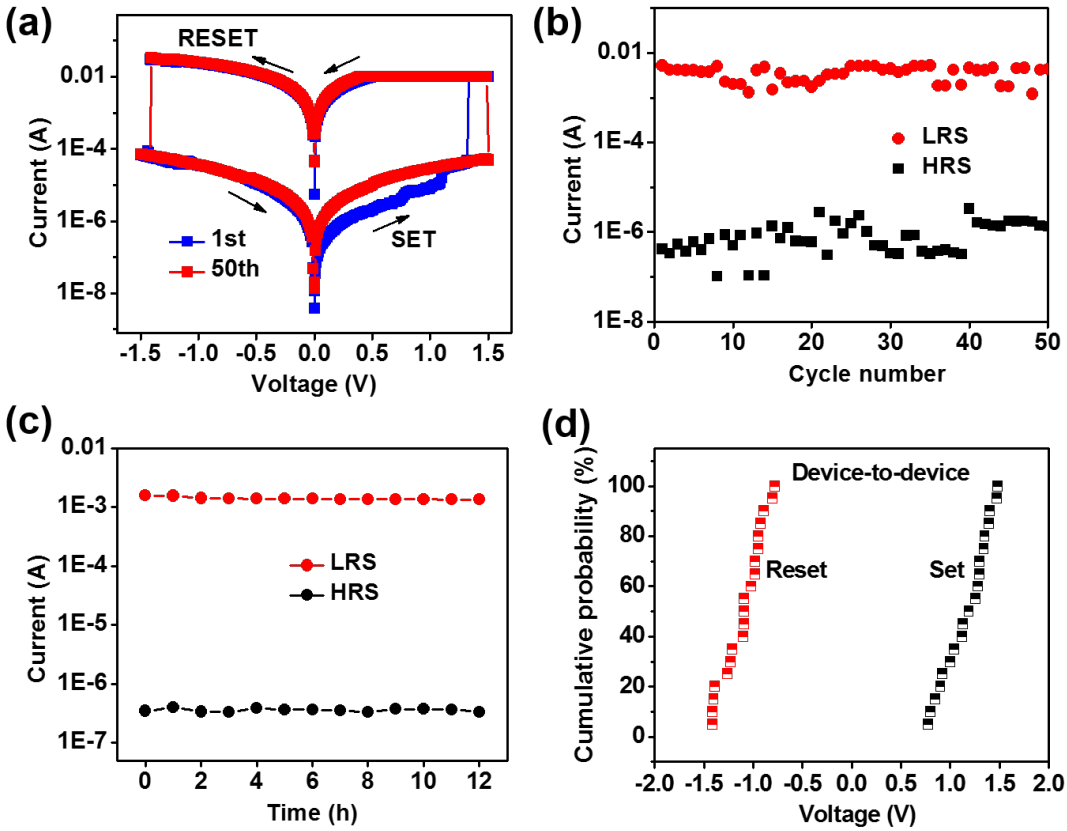

Figure 2. (a)The I-V characteristics of electrical switching behavior of perovskite based memory. (b) Cyclic tests for 50 cycles (c) Electrical reliability test for 12 h before and after electrical switching, showing no obvious degradation in HRS and LRS. (d) Cumulative probability plots for the SET and RESET voltages.

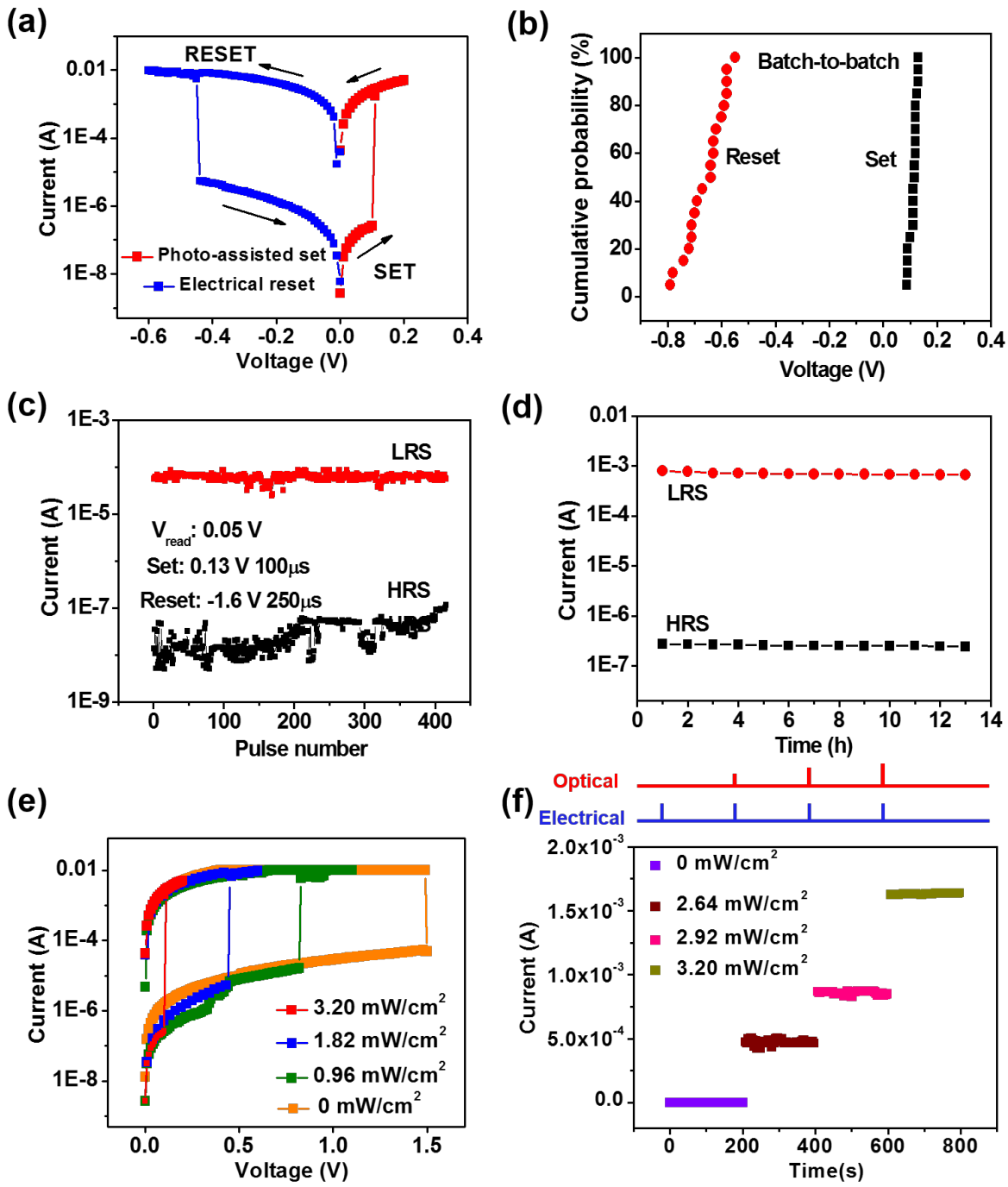

Figure 3. (a)The I-V characteristics of low-voltage photo-assisted switching behavior of perovskite based memory. The SET process is conducted under the white light illumination with a power density of 3.20 mW/cm^2. The perovskite based memory then is RESET under the dark condition. (c) Pulse switching endurance and (d) retention test for two resistance states. The pulse

condition for HRS is 0.13 V for 100 μs with white light illumination (3.20 mW/cm^2) and for LRS is −1.6 V for 250 μs. The readout voltage is 0.05 V. (e) The SET processes under different light intensities. (f) Light-intensity controlled multiple resistance states. The voltage pulse for the set processes is 0.13 V for 100 μs. The duration of optical pulses used is 1s.

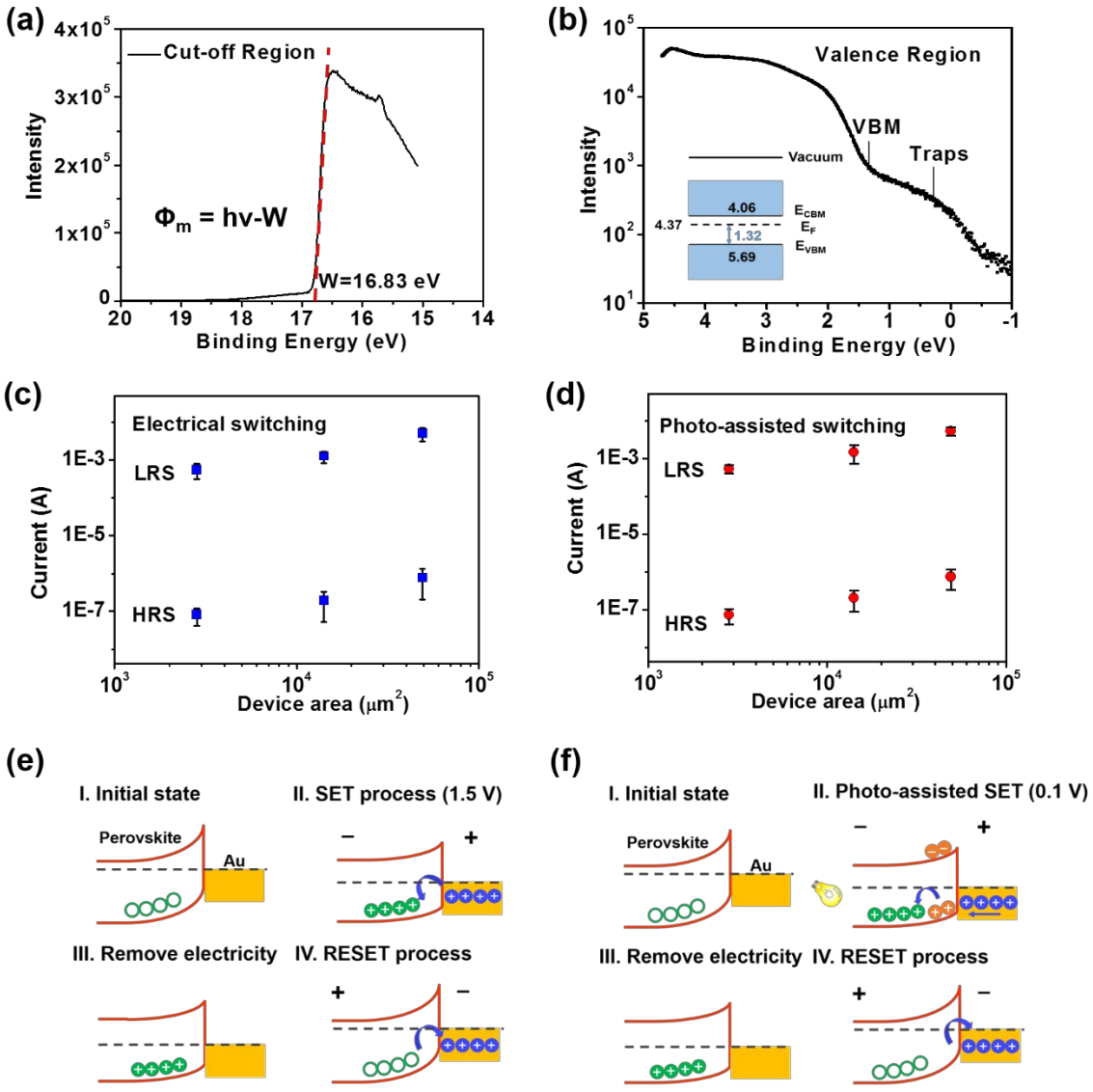

Figure 4. UPS spectra of perovskite thin film on FTO glass at (a) cut-off region and (b) valence band region obtained with *hv* =21.2 eV. The binding energy is referred to the Fermi level. The work function is determined as 4.37 eV from the intercepts. A broad distribution of hole traps is observed above the valence band edge. The difference between valence band and Fermi level can be determined as 1.32 eV. The band diagram of perovskite film is schematically illustrated in the inset of Figure 4(b). Variation of resistances at ON and OFF states of perovskite memory devices with different effective areas for (c) electrical switching and (d) photo-assisted switching. (e)

electrical switching and (f) photo-assisted switching mechanism including four states: I. initial state corresponding to HRS: hole trapping centers locate at the perovskite surface; II. SET process: hole trap states are filled, shifting the Fermi level to the valence band; III. remove light electricity: a lowered barrier and quasi ohmic contact are resulted corresponding to LRS and (d) electrical reset: holes are extracted from the trap states and a transition from LRS to HRS occurs.

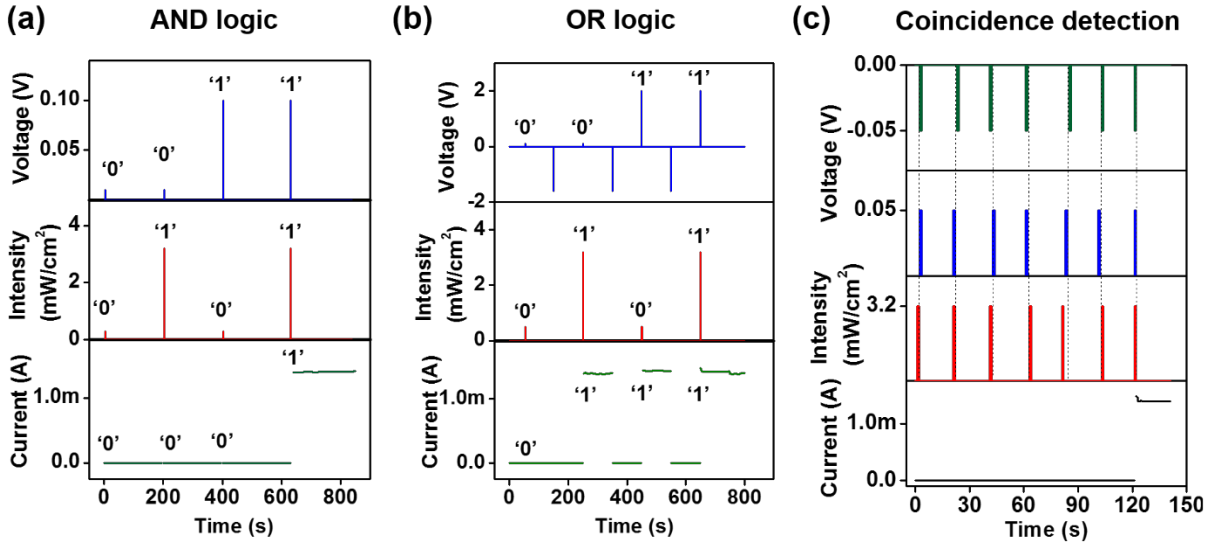

Figure 5. Demonstrations of logic operations and coincidence detection of the perovskite based memory. (a) A demonstration of AND logical operation. We defined the light pulse (>3.2 mW/cm^2, 1 s) as logic '1', light pulse (<0.3 mW/cm^2, 1 s) as logic '0', electrical pulse (0.13 V, 100 μs) as logic '1' and electrical pulse (0.01 V, 100 μs) as logic '0'. (b) A demonstration of OR logical operation. we define the light pulse (3.2 mW/cm^2, 1 s) as logic '1', light pulse (0.5 mW/cm^2, 1 s) as logic '0', electrical pulse (2 V, 250 μs) as logic '1' and electrical pulse (0. 1 V, 100 μs) as logic '0'. HRS and LRS are defined as logic '1' and logic '0' in both AND and OR logic operations. (c) A demonstration of 3-pulse coincidence detection. Three input pulses are optical pulse (3.2 mW/cm^2, 1s), electrical pulse applied to the top electrode (0.05 V, 1s) and electrical pulse applied to the bottom electrode (-0.05 V, 1s). The output current Y can represent the coincidence of the

three input pulses. Only in the case that the three pulses appear coincidently, there shows an output current corresponding to the LRS of the memory device.

TOC

An optoelectronic $CH_3NH_3PbI_{3-x}Cl_x$ perovskite resistive switching memory is designed and fabricated. The memory cell exhibits low operation voltage of 0.1 V with the assistance of light illumination, long-term retention and light sensing properties, and can perform logic operation by inputting electrical and optical signal. This device provides possibilities in reducing the complexity in smart sensor design for IoT application.

Perovskite, resistive switching memory, optoelectronic memory, logic operation, smart sensor

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Low-Voltage, Optoelectronic $CH_3NH_3PbI_{3-x}Cl_x$ Memory with Integrated Sensing and Logic Operations