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Monolithic integration of all-in-one supercapacitor for three-dimensional electronics

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((Optional Dedication))

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Abstract- Supercapacitor is usually stacked in the configuration of layered sandwiched architecture, and has been adopted as discrete energy storage device or circuit component. However, this stacked structure decreases mechanical integrity, leads to low specific capacity, and prevents high-density monolithic integration. Here we fabricated all-in-one supercapacitors by integrating cathode, anode, current collector and separator into one monolithic glass fiber (GF) substrate together with other circuit components through matured and scalable fabrication techniques, and embedded the all-in-one supercapacitor as a component for three-dimensional (3D) electronics. This all-in-one architecture demonstrated its effectiveness in the

prevention of the delamination of the sandwiched supercapacitor and the minimization of the proportion of inactive materials. The supercapacitor delivers high power density (320 mW cm^{-3}) and energy density (2.12 mWh cm^{-3}), and exhibits a capacitance retention of 100% even after a continuous cycling of 431 hours. Furthermore, we construct a 3D polydimethylsiloxane/GF architecture for driving a flash light emitting diode system, where the all-in-one supercapacitor is monolithically integrated in the 3D system, and each layer is connected via vertical through-holes. This all-in-one device can be constructed with a macroscopically available membrane and readily integrated into 3D systems without secondary packaging, providing the potential for high-density heterogeneous 3D electronics.

1. Introduction

The development of electronics requires heterogeneous integration for multiple functionalities. Three-dimensional (3D) integration enables short interconnection distance and more compact size.[1-5] As an energy storage device and circuit element, supercapacitor has been widely investigated in the last two decades as a discrete component.[6-10] State-of-the-art supercapacitors predominantly present sandwiched architecture, where current collector, cathode, separator and anode are separately prepared and then assembled by stacking.[6-7, 11-12] This discrete stacking approach increases weight and volume, and decreases mechanical integrity, leading to a low gravimetric or volumetric capacity.[13-14]

All-in-one supercapacitors enable monolithic integration of all of the components into one substrate, which can drastically minimize the proportion of inactive material and avoid the possibility of multilayer delamination.[13-15] The substrates for the all-in-one supercapacitor can act as the separators simultaneously, where two sides of the

substrate are metallized to form a conductive/non-conductive/conductive sandwiched structure.[14, 16-17] The conductive layer displays a 3D framework structure, which can facilitate efficient ion/electron transportation. In the previous works, different 3D porous sheets, such as paper,[14] nylon membrane,[14] hydrogel[17] and polypropylene[16] films, have been utilized as the substrates. Various conducting polymers, including PEDOT, PANI and PPY/GO, were exploited as the active materials to fabricate the symmetrical devices. These prototypes demonstrate a conceptual all-in-one architecture and show superior electrochemical performance. To increase working potential window, the construction of asymmetrical supercapacitor with different cathode and anode materials is a normal route to enlarge the potential window and boost the power density.[18-19] Among the electrode materials, two-dimensional (2D) materials were intensively studied for their high theoretical capacitance due to their large specific surface area (SSA) and abundant electrochemical active sites.[6-7, 19-21].

To realize high integration level for future electronics, advanced three-dimensional (3D) electronic packaging is a promising technology. To enable this function, it requires fine traces and tight substrates, and small through holes in 3D system. Recently, embedded components (including capacitors and resistors) have been integrated into substrates to achieve a product miniaturization with short interconnection distance.[22-23] Supercapacitors have not been integrated into 3D electronic system because of the fundamental issues of architecture design and processing compatibility.[2]

In this work, we describe the fabrication of an all-in-one supercapacitor (**Figure 1**), which is further embedded into polydimethylsiloxane/glass fiber (PDMS/GF) membrane substrates for driving a 3D electronic system. The GF is selected as the all-

in-one substrate due to its high SSA (2.73 m^2 g^{-1}) and proper pore distribution. The supercapacitor exhibits an areal capacitance of 340.6 mF cm^{-2} at a scan rate of 1 mV s^{-1}, and delivers maximum power and energy densities of 320 mW cm^{-3} and 2.12 mWh cm^{-3}, respectively. After a very short charging of 10 s, the 3D system can continuously work more than 5 min. This all-in-one architecture enables the integration of all the discrete components, which allows highly mechanical integrity and intimate interface between the separator and electrode.[14]

2. Results and discussion

2.1 Structural and morphological characterization of the electrodes

Figure S1 shows a photo of large-scale metallized GF membranes after sputtering Ni. To optimize the conductivity and pore size of the conductive network, different current density and deposition time of the Ni electrodeposition process were applied (Figure S2-S5). The final applied current density was determined as 10 mA cm^{-2} with a deposition duration time of 20 min. The SEM images of GF substrates before and after Ni deposition (Figure S6) show that the fibers enlarge and intertwine with each other after the metallization, which leads to a dramatically decrease in the sheet resistance of the substrates (from 20 to 0.098 Ω $□^{-1}$). After the Au plating, the sheet resistance of all-in-one current collector reduces to 0.09 Ω $□^{-1}$.

Figure S7 shows optical photos of the all-in-one supercapacitor. The cross-sectional SEM image of the supercapacitor (**Figure 2a**) shows a tight adhesion of the electrodes to the GF substrate (separator). Figure S8 is cross-sectional SEM image of the supercapacitor after drying. The MnO_2 cathode was electrochemically deposited onto one side of the all-in-one sandwiched structure. Figure S9 shows the SEM images of the samples with different duration time. With the increase of deposition time, the diameter of the fibers obviously enlarges, and the MnO_2 layer gradually

connects together. Figure 2b is a sample after the deposition of MnO_2 for 10 min, showing a uniform distribution and crosslinking characteristics of the fibers. This structure also leaves sufficient macro-pores for ion transport. The surface of the MnO_2 layers (Figure 2c and S10) displays a morphology of nanosheets, increasing the SSA and electrochemical active sites of the electrode.[24] High-resolution TEM image of the MnO_2 cathode (Figure 2d) shows two typical lattice spacing of 0.244 nm and 0.212 nm, corresponding to the selected area electron diffraction (SAED) pattern result (Figure S11). The XRD pattern (Figure 2e) shows broad diffraction peaks at 36.7°, 42.1°, 55.6° and 65.9°, which can be indexed as the lattice planes of (100), (101), (102) and (110) of the ε-MnO_2.[25] The full XPS spectrum of MnO_2 (Figure S12) contains typical Mn and O elemental spectra in the binding energy areas of 635-660 eV and 526-536 eV. High-resolution Mn 2p spectrum (Figure 2f) shows two pair of typical peaks, belonging to Mn^{4+} and Mn^{3+}.[25] The peaks, located at 654.1 eV and 642.5 eV with a spin-energy separation of 11.6 eV, are the characteristic spin−orbit peaks of Mn 2p1/2 and Mn 2p3/2, respectively. The presence of three deconvoluted peaks in the O 1s spectrum (Figure S13), at the binding energies of 530.1 eV, 531.0 eV and 532.2 eV, represents the O^{2-}, OH^- and the H_2O.[25]

The anode is prepared by vacuum filtration of the holey reduced graphene oxide/carbon nanotube (HrGO/CNT) composite onto the other side of the all-in-one sandwiched structure. The HrGO nanosheets stack together in a nearly parallel manner with CNTs intercalate among the layers, as shown in the cross-sectional SEM images (Figure 2g and S14). TEM image of GO (Figure S15) shows an intact nanosheet structure, which is etched by H_2O_2 to form holes that randomly distribute in the sheet (Figure 2h). The diameter of multi-walled CNTs ranges from 5 nm to 20 nm (Figure 2i). The holes in HrGOs (with the size of 10-50 nm) and pores (in the range of

5-20 nm) formed by the intercalation of CNTs are within the scope of mesopores, which contributes to improve the capacitive performance of the anode due to its superior SSA and short electrons/ions transport pathways.[26] From the perspective of ion kinetics, the holes in HrGO facilitate the migration of ions in the vertical direction, while the CNT framework inside the HrGO layers benefits the transportation of ions in the horizontal direction.[27-28] Figure S16 presents the Raman spectra of GO, holey GO (HGO), acidified CNT (CNT-COOH) and HrGO/CNT, respectively. The I_D/I_G ratio in HGO and HrGO/CNT is slightly higher than that of GO, possibly a result of additional defects and oxygen functional groups during the generation process of the nanopores in HrGO.[29]

2.2 Electrochemical characterization of the cathode and anode

Figure S17a shows the areal capacitance of the MnO_2 cathode with different deposition time, calculated from the cyclic voltammetry (CV) curves at the scan rates of 1-10 mV s^{-1}. The samples with high mass loading of MnO_2 show a relatively inferior rate performance, because thick active material leads to a long electron transfer path and blocks the channel for ion transport.[30] This phenomenon is corresponding to the electrochemical impedance spectroscopy (EIS) results (Figure S17b), where the internal resistance of the samples enlarges as the deposition time increases. The shape of CV curves (Figure S17c) shows that the rectangularity decreases as the deposition time increases, which is also an evidence for the degradation of rate performance. Although the areal capacitance plot of the samples at the scan rate of 1 mV s^{-1} (Figure S17d) shows a peak value at the deposition time of 20 min, we select the sample with the 10-min deposition of MnO_2 for assembling the all-in-one supercapacitor because of the trade-off between the capacitance and the rate performance.[31]

Figure 3a and Figure S18a are the CV curves of the cathode at scan rates ranging from 1 to 100 mV s^{-1}. The CV curve of the cathode shows a typical rectangle-like shape because of the essential reversible successive surface redox reactions of MnO_2 active material.[32] Its areal capacitance reaches 675 mF cm^{-2} at the scan rate of 1 mV s^{-1} (Figure S18b), and the value decreases accordingly with the increase of the scan rate, while it can maintain a retention of 52% even when the scan rate increases by 20-fold (Figure S18b). The galvanostatic charging/discharging (GCD) characteristics (Figure 3b and Figure S18c) are investigated in the range of 0.5-20 mA cm^{-2}. There are no voltage plateaus in the curves, which is consistent with the CV results. All the curves show standard isosceles triangle shapes, illustrating negligible self-discharge of the electrode during the charge-discharge cycle, a typical feature of capacitive behavior. The frequency response analysis at an open-circuit potential, in the range of 0.01Hz - 100 kHz with an amplitude of 5 mV, was used to investigate the alternating current impedance of the electrode. The equivalent series resistance (ESR) calculated from the Nyquist plot (Figure S18d) is only 3.6 Ω, indicating an excellent ionic response of the electrode. The cycling stability of the electrode is studied by repeating CV test at the scan rate of 20 mV s^{-1} (Figure 3c). There is a temporary rise in the capacitance at the beginning, and the value reach a peak at the 6,000th cycle, which likely to be resulted from the wetting process of fully penetration and the gradual formation of stable interface between the electrode and electrolyte.[33] It is noteworthy that the capacitance retention can be 91.3% even after a successive test of 20,000 cycles, indicating a superior stability of the electrode. In addition, the electrochemical properties of the sample with 5-min and 20-min deposition are also systematically investigated (Figure S19 and S20). The high performance of the cathode is due to its high conductivity and hierarchical nanostructure, which allows fast electron

transportation through the conductive networks, unimpeded ion transport through the micrometer channels over long distance, and large SSA for providing more electrochemical active sites.[34-35]

The electrochemical performance of the carbon-based anode is also investigated. CV curves in the range of 1-100 mV s^{-1} (Figure 3d and Figure S21a) show typical electric double layer shapes.[32] The areal capacitance of anode is 592 mF cm^{-2} at the scan rate of 1 mV s^{-1}, which can keep as 463.7 mF cm^{-2} when the scan rate reaches 20 mV s^{-1} (Figure S21b). The GCD curves (Figure 3e and Figure S21c) from 0.5 to 20 mA cm^{-2} show a shape of typical isosceles triangle, owing to the excellent ion and electron transporting property during the electrode. This phenomenon can be also explained by the EIS plot (Figure S21d), which illustrates a low equivalent series resistance of 3.8 Ω. The anode exhibits a capacitance retention of 103% even after a long cycling of 50,000 times at the current density of 10 mA cm^{-2} (Figure 3f). The high electrochemical performance of the anode is due to the formation of mesopores among all-carbon electrode, where the CNTs intercalate in the HrGO framework along the horizontal direction and the pores in HrGO line up along the vertical direction.

2.3 Electrochemical characterization of the all-in-one supercapacitor

The all-in-one supercapacitor was assembled by matching the capacitance of the cathode and anode. Its working potential window was determined as 1.6 V. The CV curves of the supercapacitor with a wide scan rate range of 1-100 mV s^{-1} are shown in **Figure 4a**. The areal capacitance (Figure 4b) reaches 340.6 mF cm^{-2} at the scan rate of 1 mV s^{-1}. The value maintains as 200 mF cm^{-2} when the scan rate increases to 10 mV s^{-1}, and the capacitance retention is 42.1% at the scan rate reaches 50 mV s^{-1}, verifying the high rate performance of the supercapacitor. The GCD curves (Figure 4c

and 4d) show the similar shapes as the single electrodes at all tested current densities, demonstrating a pure capacitive behavior of the supercapacitor. These results are due to the free electrons and ions transport among of the electrodes. After a successive cycling test (431 hours, 12,500 cycles) at the current density of 5 mA cm^{-2} (Figure 4e), the supercapacitor shows a capacitance retention of 100.1%, demonstrating long-time stability. The frequency response analysis is conducted to investigate the intrinsic impedance of the supercapacitor. The ESR is as low as 7.0 Ω (Figure 4f), which suggests high charge-transfer behavior and electrochemical response at the interface between the electrolyte and the electrode at the high-frequency range. Furthermore, the nearly vertical line in the low frequency also indicates an ideal capacitive behavior of the supercapacitor.[36]

To evaluate the electrochemical performance of our device, Figure 4g and 4h list the energy and power densities of recently reported all-in-one supercapacitors, respectively. These supercapacitors including PAN-PCH 0.5,[16] PAN-PCH 0.1,[16] PAN-PCH 0.05,[16] NM-PEDOT,[14] FP-SC-PEDOT,[14] PPy-GO//PPF700,[17] and PPy-GO//PPF1000.[17] The Ragone plot calculated by the areal parameters (Figure 4g) shows that the electrochemical values of our device are on the top right corner of the figure. Our supercapacitor can deliver a tested maximum E_a of 106.2 μWh cm^{-2} at the P_a of 400 μW cm^{-2}, and maintains an E_a value of 22.9 μWh cm^{-2} at the tested maximum P_a of 16,000 μW cm^{-2}. From the volume perspective (Figure 4h), the parameters of our device are slightly lower than NM-PEDOT, comparable to PF-SC-PEDOT, and at least 5 times larger than the counterparts. Even calculated based on the volume of the full device, our device can show maximum E_v and P_v of 2.12 mWh cm^{-3} and 320 mW cm^{-3}, respectively. Some key parameters of recently reported supercapacitors, including C_a, C_V, working potential and cycle stability, are listed in

Table S1. Our device exhibits one of the highest C_a and C_V values, and shows the best cycling stability and largest working potential window. To further improve the energy and power densities of our device, the proportion of active material in the supercapacitor should be increased by loading more active materials or decreasing the thickness of the separator.

2.4 Structural characterization and demonstration of the 3D system

We design a 3D electronic system as a four-layer circuit layout with an all-in-one embeded supercapacitor (**Figure 5a**), to generate a clock signal for adjusting the flash frequency of three red light emitting didoes (LEDs). Exploded diagram of the fabricated 3D electronics (Figure 5b) shows the design details, which is built layer-by-layer and vertically interconnected by through-holes (the dash lines in Figure 5b). The top layer (Figure 5c) hosts most of the functional components, including resistors, capacitors, diodes, chips, switches and LEDs. The second and third layers, mainly acting as the current collectors of the cathode and anode of the all-in-one supercapacitor, are simplified as two pads that interconnected with the top layer. The bottom layer functionalizes as the traces for the interconnection of the 3D system.

The fabrication process of the 3D system based on the PDMS/GF package substrate (Figure 5d and Figure S22) involves the integration techniques, including routing, interconnecting, bonding and packaging. Compared to pure PDMS substrate, the involvement of GF membrane notably increases the mechanical strength.[37-38] As a result, there is a fivefold increase of the tension strength from PDMS to PDMS/GF (Figure S23). Furthermore, even after all the layers are mounted onto the substrate, the 3D system based on PDMS/GF still presents a certain extent of flexibility (Figure S24).

Figure 5e and Figure S25 show top-view optical microscopy images of part of the circuit diagram from the top layer, which typically contain the insulation area, pads, traces, through-holes and ground. The insulation boundary with a width of about 1 mm is for isolating the ground and the conductive circuit. The pad is used for mounting the functional components into the circuit. The trace is designed for in-plane electrical connection. Figure 5f shows the cross-sectional optical microscopy schematic of the through hole, fully filled with cured silver paste to realize the interconnection between layers.

The all-in-one structured device can be fabricated by macroscopically available membrane without secondary packaging.[39] Two pieces of these supercapacitors in series were then integrated in the PDMS/GF package substrate as embeded devices to power the flash LED circuit. The signals of the timing chip (SA555D) and decade counter chip (CD4017B) in the circuit (Figure 5g) are tested by an oscilloscope (KEYSIGHT 33522B). The frequencies of the timing chip and decade counter chip in this work are 7.35 Hz (0.136 s for one cycle) and 0.69 Hz (1.45 s for one cycle), respectively, which can be regulated by the resistances and capacitors in the circuit. The working 3D system is shown in video S1, and the screenshot of one cycle (from 16.33 s to 17.83 s) is shown in Figure 5h. After charging the supercapacitor for 10 seconds, the 3D system can continuously work for more than 200 cycles (5 min).

3. Conclusion

In summary, we prepared an embedded all-in-one supercapacitor for the demonstration of driving a 3D flash LED system. The supercapacitor was fabricated by optimizing the fabrication route with matured techniques, such as, sputtering, electroless plating, electrodeposition, and vacuum filtration. The all-in-one architecture of the supercapacitor can drastically minimize the proportion of inactive

material and avoid the possibility of multilayer delamination. It can exhibit much superior electrochemical performance than the recently reported counterparts. The 3D electronics was fabricated by solving the critical and fundamental issues, such as architecture design and processing compatibility. The supercapacitor can be readily embedded into high integration system without secondary packaging. These above-mentioned approaches are highly reliable and show great potential for practical applications of 3D system in the future.

4. Experimental Section

Metallization of the GF membrane substrate: A thin Ni layer was sputter-deposited onto near surfaces of the GF film (thickness of 260 μm) to metallize the non-conductive substrate (Figure 1a). The depth of the Ni layer penetrated into the GF membrane is approximately 30 μm with the deposition time of 30 min. The conductivity can be further increased by electrochemical-plating Ni (Figure 1b). The solution was prepared by adding 260 g $NiSO_4 \cdot 6H_2O$, 40 g $NiCl_2 \cdot H_2O$ and 0.2 g sodium dodecyl sulfate (SDS, anionic surfactant) into 1 L (deionized) DI water. The pH value of the solution was adjusted to 4.8 by $NH_3 \cdot H_2O$. The procedure of electroless plating Au was given in the previous paper (Figure 1c).[40] After the Au plating, the obtained samples were washed and dried.

Fabrication of the all-in-one supercapacitor: The anode was fabricated by vacuum filtering holey reduced graphene oxide (HrGO) and multiwalled carbon nanotube (MWCNT) composite (Figure 1d). The preparation of holey GO (HGO) was obtained according to chemical etching method reported previously.[29] Typically, fewer layer GO (Suzhou Hengqiu Tech. Inc.) powder was dissolved into DI water to

obtain a 2 mg mL^{-1} aqueous suspension solution. 100 mL of the GO solution was mixed with 10 mL H_2O_2 solution (30 v/v%) and heated to 95 ºC under stirring. After the reaction for 4 hours, a piece of Pt foil was placed into the solution to decompose the residual H_2O_2.[41] Acidified CNT (CNT-COOH, Suzhou Tanfeng Tech. Inc.) powder was then dissolved into the above-obtained HGO solution to obtain an HGO/CNT composite suspension solution (HGO, 0.25 mg mL^{-1}; MWCNT, 0.06125 mg mL^{-1}). 350 uL $NH_3 \cdot H_2O$ (28 wt%) and 18 uL hydrazine hydrate (98 wt%) were added into 100 mL HGO/MWCNT solution, which was then heated to 95 ºC and kept for 1 h without stirring. The solution was vacuum filtered onto the current collector (with an area of 4 cm^2) to obtain the anode (thickness of ca. 40 μm).

The growth of 2D MnO_2 cathode material was conducted onto the other side of the all-in-one substrate by electrochemical deposition technique (Figure 1e).[25] Specifically, the precursor solution for MnO_2 deposition was prepared by adding $Mn(Ac)_2$ into DI water to obtain a 0.1 M aqueous solution. The solution was heated and kept at 60 ºC. The deposition was conducted using a constant current technique of 10 mA cm^{-2} in a two-electrode system. The deposition duration time was from 5 min to 30 min.

Integration of the all-in-one supercapacitor into 3D electronics: The PDMS silicone elastomer (Sylgard 184, DOW CORING) was chosen as the substrate and the package material. The base and curing agents were mixed with a weight ratio of 10:1. A few pieces of GF membranes were placed into the resin to enhance the mechanical strength of the obtained PDMS/GF substrates (Figure $5a_i$). Two thin Cu foils (8 μm) were laminated onto both sides of one PDMS/GF membrane, which was then cured for 12 h at 60 ºC (Figure $5a_{ii}$).

The traces, pads and through-holes were fabricated by high power laser (Figure 5a$_{iii}$; HAN's laser EP-15-DW, wavelength of 355 nm, highest scanning line speed of 4 m·s^{-1}). All of the electronic components (resistors, capacitors, diodes, triodes, chips, switches and LEDs) were surface mounted onto the board by silver paste (Figure 5a$_{iv}$). The supercapacitors were placed between two substrates with reserved pads and then packaged by PDMS. The via holes were filled by silver paste (Figure 5a$_{vi}$).

Materials and device characterizations: The morphology and architecture were characterized by scanning electron microscopy (SEM, SUPRA 55, ZEISS, Germany) and high-resolution transmission electron microscopy (HR-TEM, JEM 2100F, JEOL, Japan). The elemental and structural analysis were characterized by X-ray photoelectron spectroscopy (XPS, PHI 5000 Versaprobe II, Ulvac-Phi, Japan) and X-ray diffraction (XRD, D8 Advance, Bruker, Germany), separately. The mechanical strength of the PDMS and PDMS/GF samples were tested on an electronic universal testing machine (CMT6104, Skyan, China).

The electrochemical performance of the cathode, anode and device, including cyclic voltammetry (CV), galvanostatic charging/discharging (GCD) and electrochemical impedance spectroscopy (EIS), was investigated by an electrochemical workstation (VMP3, Bio-Logic, France). The electrochemical property of cathode and anode is characterized in a 3-electrode cell configuration, where neutral 0.5 M Na_2SO_4 aqueous solution is the electrolyte, a Pt foil is the counter electrode, and a standard saturated calomel electrode (SCE) is the reference. The working potential windows of the cathode and anode are determined in the range of 0-0.8 V and -0.8-0 V, respectively, where the electrodes exhibit a purely capacitive behavior and show no obvious polarization.[32]

Supporting Information ((delete if not applicable))
Supporting Information is available from the Wiley Online Library or from the author.

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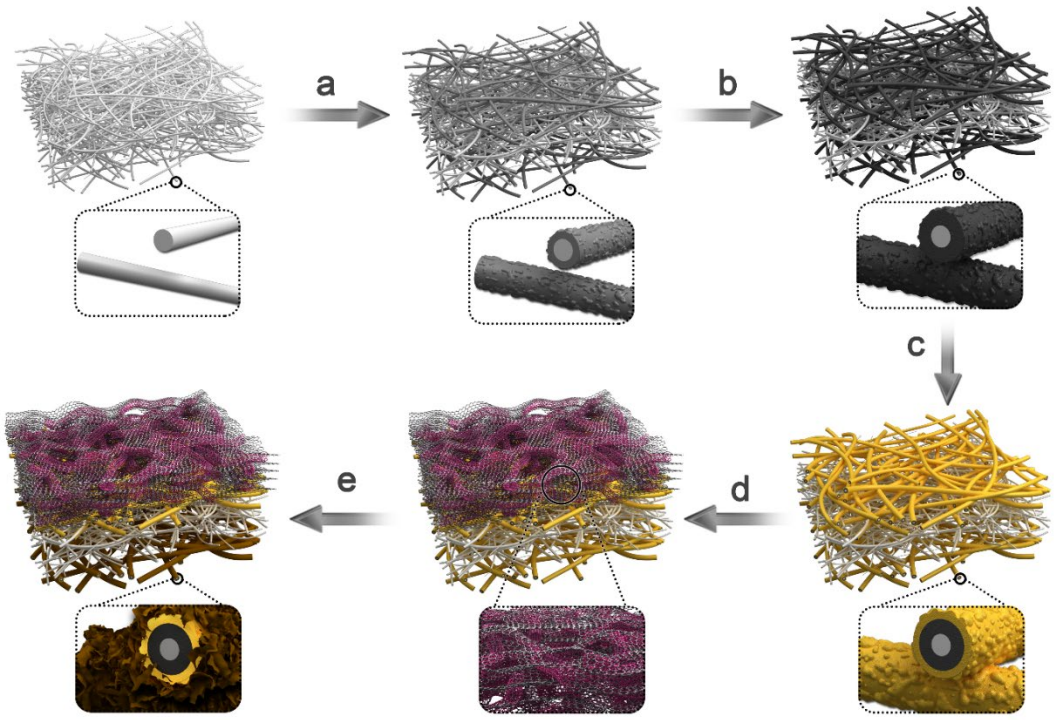

Figure 1. Schematic illustration of the preparation process of all-in-one supercapacitor: (a) Sputtering Ni onto near surfaces of both the upper and lower sides of the GF film, leaving the middle part as the separator. (b) Electrochemical plating of Ni to enhance the conductivity of the current collector. (c) Electroless plating of Au to protects the Ni layer during the electrochemical reaction. (d) Vacuum filtering a film of HrGO/CNT onto one side of the substrate as the anode. (e) Electrodepositing a layer of MnO_2 onto the other side of the substrate as the cathode.

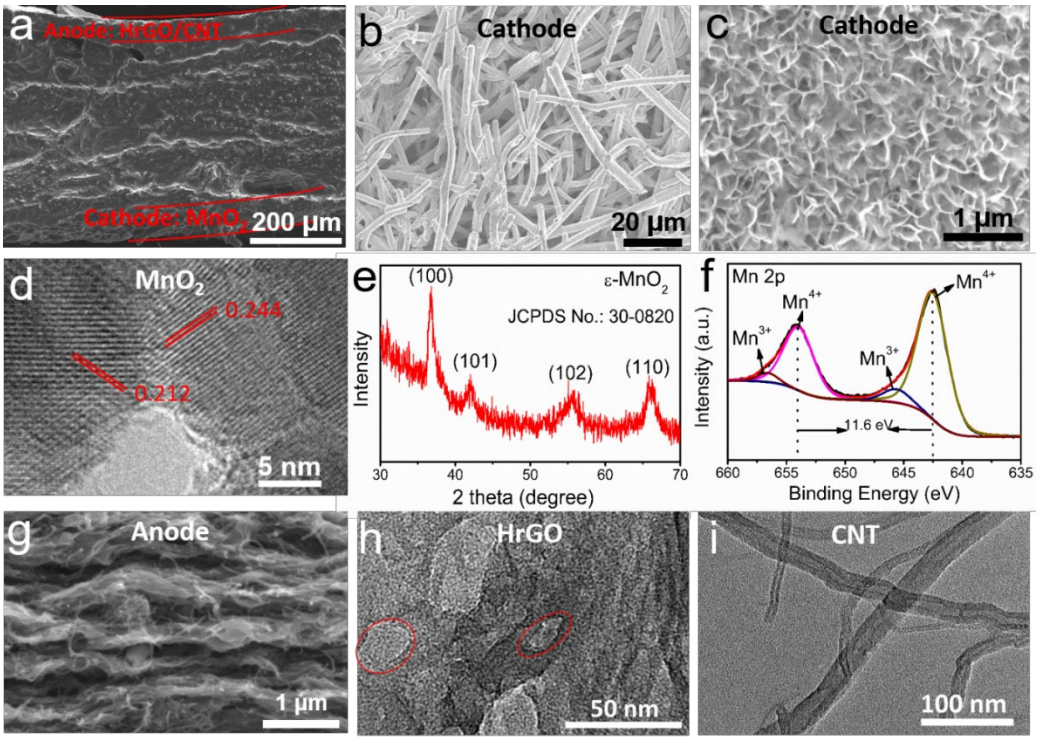

Figure 2. Structural and morphological characterization of the all-in-one supercapacitor. (a) Cross-sectional SEM image of supercapacitor. (b)-(f) Low-magnitude SEM, high-resolution SEM, HRTEM image, XRD spectrum and Mn 2p XPS spectrum of the MnO_2 cathode. (g) Cross-sectional SEM image of the HrGO/CNT anode. (h)-(i) HRTEM images of HrGO and CNT, respectively.

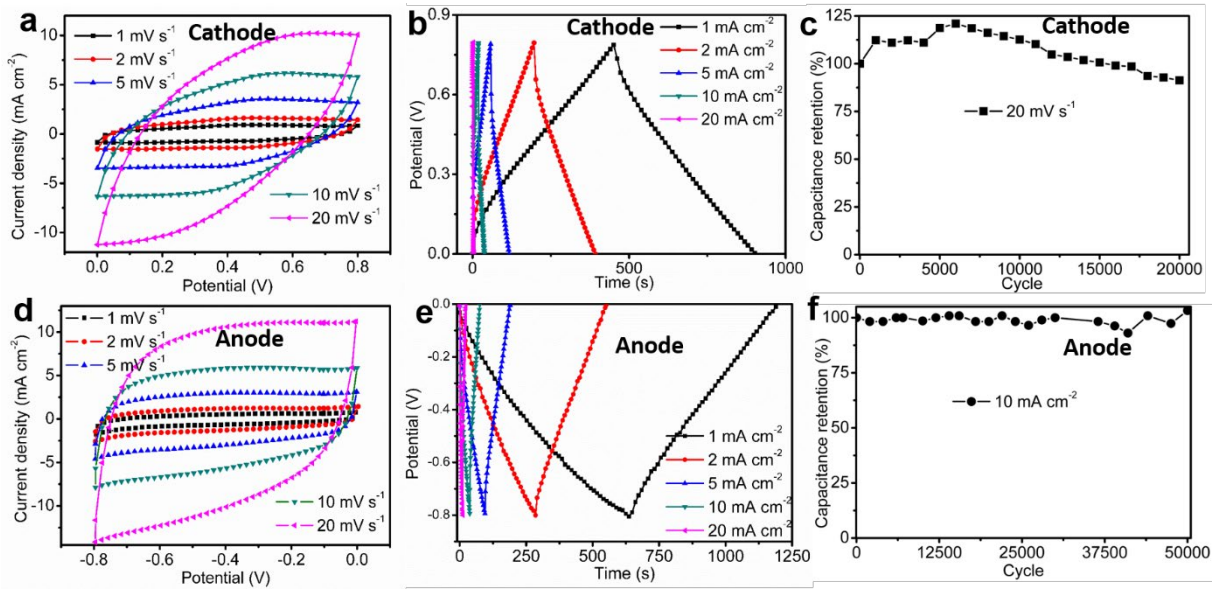

Figure 3. Electrochemical performance of the cathode and anode. (a) and (d) CV curves of the cathode and anode at the scan rate of 1-20 mV s^{-1}. (b) and (e) GCD curves of the cathode and anode at the current densities ranging from 1 to 20 mA cm^{-2}. (c) Cycling stability of the cathode at the scan rate of 20 mV s^{-1}. (f) Cycling stability of the anode at the current density of 10 mA cm^{-2}.

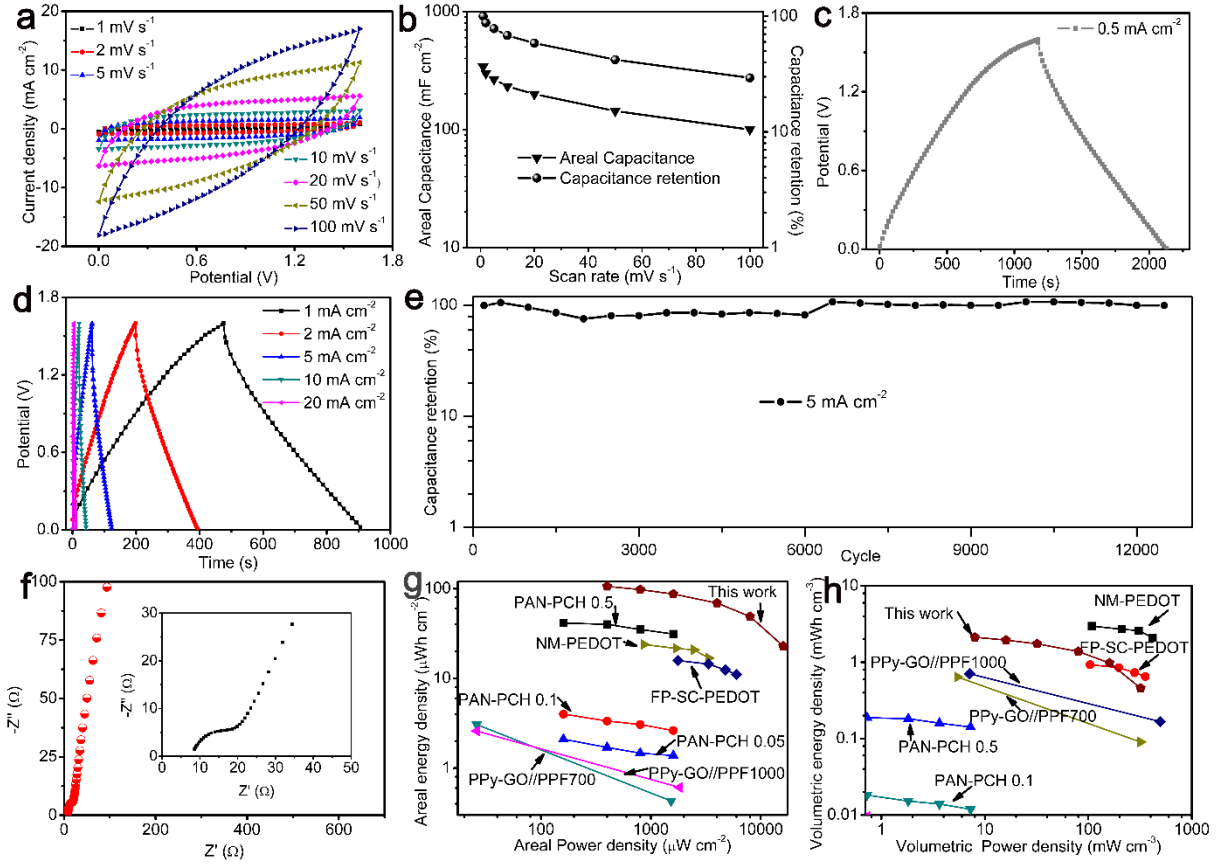

Figure 4. Electrochemical performance of the all-in-one supercapacitor. (a) CV curves at scan rates ranging from 1 to 100 mV s^{-1}. (b) Variation of the areal capacitance and capacitance retention as a function of scan rate calculated by the CV study. (c)-(d) GCD curves with the current densities of 0.5-20 mA cm^{-2}. (e) Cycling stability characterization at the current density of 5 mA cm^{-2}. (f) Nyquist plot of the device. (g) and (h) Ragone plots of our supercapacitor as compared to recently reported all-in-one ones.

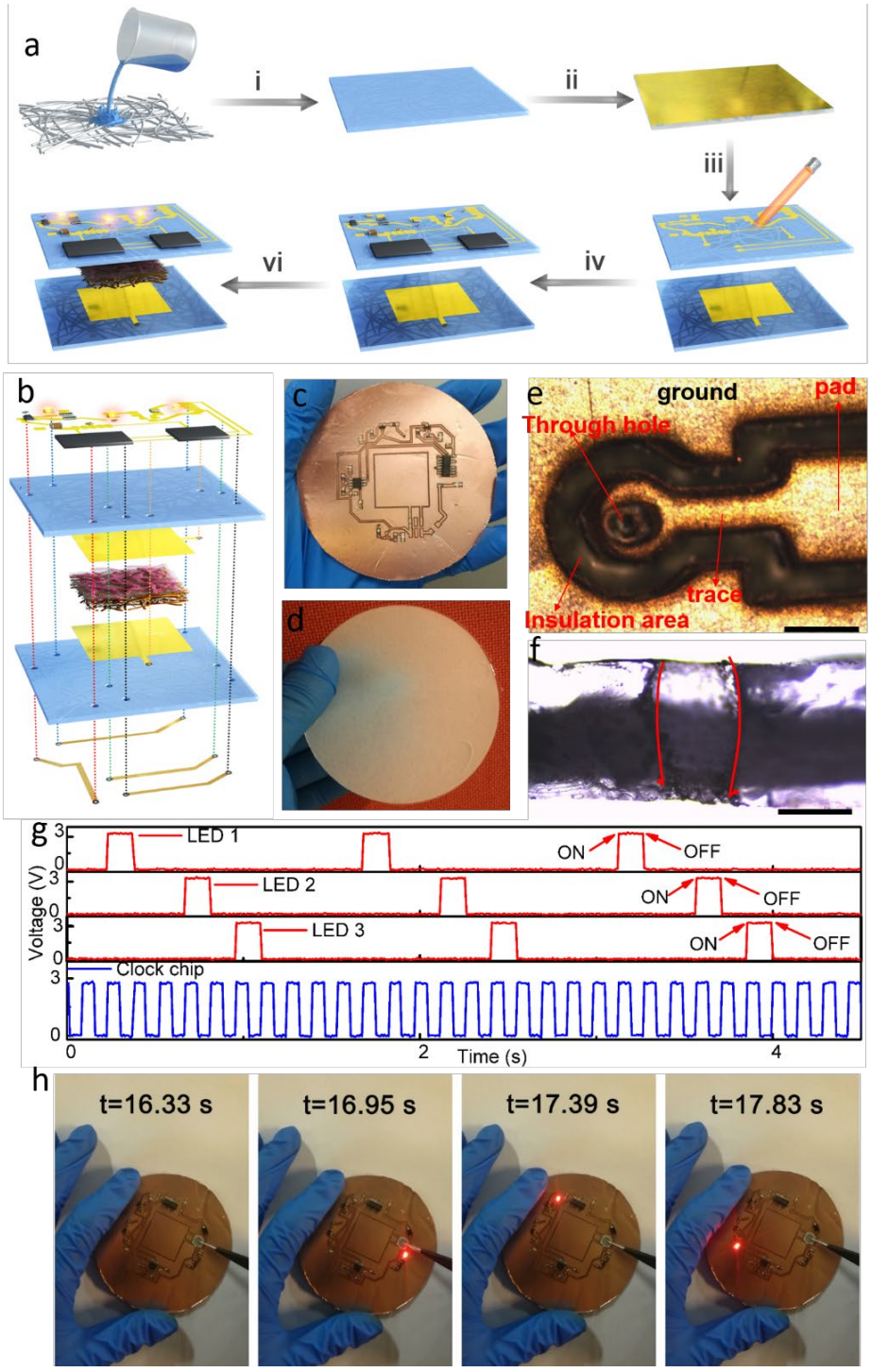

Figure 5. Fabrication, structural characterization and demonstration of the 3D electronics. (a) Schematic illustration for fabricating the 3D system powered by all-in-one supercapacitor: (i) Fabrication of the PDMS/GF substrate; (ii) Lamination of Cu foil onto the PDMS/GF substrate; (iii) Sculpturing circuit diagram and through-holes in the substrate by high-power laser ablation; (iv) Mounting the electric components onto the substrate; (vi) Embedding the all-in-one supercapacitor into the substrates and realizing the interconnection to form the 3D system. (b) Exploded diagram of the fabricated 3D electronics. (c) Top-view photo of the sample. (d) Photo of the PDMS/GF substrate. (e) Top-view optical microscopy image of part of the circuit diagram, scale bar: 2 mm. (f) Cross-sectional optical microscopy image of the substrate containing a through hole, scale bar: 300 μm. (g) The signals of the timing chip and decade counter chip in the circuit. (h) Screenshot of the 3D electronics during working.

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All-in-one asymmetrical supercapacitor is prepared by integrating 2D MnO_2 cathode, holey reduced graphene oxide/CNT anode, Ni/Au current collector and separator into one monolithic glass fiber (GF) membrane. The all-in-one supercapacitror is embedded into GF/PDMS substrate to realize the integration with three-dimensional electronic system.

Keyword: all-in-one, supercapacitors, three-dimensional electronics, heterogeneous integration

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Monolithic integration of all-in-one supercapacitor for three-dimensional electronics