Pico-watt Complementary Inverter with Negative Capacitance Two-Dimensional Semiconductor Transistors

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Abstract

The increase of power consumption poses serious challenges to the performance and reliability of integrated circuits. The decrease of the operation voltage of an individual transistor can reduce power consumption, which is proportional to the square of the voltage. A fundamental limit for the supply voltage of conventional field-effect transistors is the long high-energy tail of the Boltzmann distribution of the carrier population at the source junction, which requires a gate voltage at least 60 mV to change one decade of current. Here we adopt two-dimensional semiconductors as channel materials and hafnium zirconium oxide as negative capacitance gate stack to realize low-power complementary logic inverter. By constructing van der Waals contact to improve the charge injection and control the carrier type, we achieve unipolar *p*-type WSe_2 FET with reduced hole Schottky barrier height. With HZO/Al_2O_3 NC gate stack, the WSe_2 FET shows minimum subthreshold slope of 18 mV/dec, which allows to reach the same ON-state current at a lower V_{dd} without increasing the OFF-state

current. The complementary inverter with MoS_2 and WSe_2 NCFETs shows pico-watt power consumption of 68 pW. This strategy contributes to the development of the 2D semiconductor electronics and can be also extended to other low-dimensional semiconductors for low-power electronic devices.

KEYWORDS: Two-dimensional materials; complementary circuits; steep slope; negative capacitance; low power

1. Introduction

With the development of portable electronics, the demands for low-power system have reached an unprecedented level.[1-5] The overall power consumption of a computing system is a result of the device density and the power consumption of a single device. As the density of transistors continues to increase, it becomes imperative to reduce the power consumption of an individual field-effect transistor (FET). As the thickness of the dielectric and the channel of FETs is approaching a few nanometers, electrostatic gate control of nanoscale FETs becomes ineffective, giving rise to the increase of the SS and leakage current and undesirable excessive power dissipation.[6-11] It is essential to reduce the SS and achieve efficient control of the channel for realizing low power electronic devices. However, the SS of FET is limited by the Boltzmann distribution from reaching 60 mV/dec at room temperature, and therefore precludes the reduction of the supply voltage and the overall power consumption.[3, 12-15]

Recently, negative capacitance (NC) has been proposed and demonstrated to

overcome the Boltzmann tyranny by integrating of a ferroelectric layer within the gate stack. It enables the transistor to reach the same ON-state current at a lower V_{dd} without increasing the OFF-state current due to steeper SS. Two-dimensional (2D) layered transition metal dichalcogenides (TMDs) have the potential to scale down the channel length to nanoscale and possess a lower power consumption for their effectively electrostatic control. It is highly desirable to further reduce power consumption by integrating 2D semiconductor channels and NC gate stack to form NCFETs.[3, 14, 16-18]

CMOS logic dissipates less static power than transistor-transistor logic or NMOS logic because of the low static current, and is one of the most used technologies in VLSI chips.[19, 20] The construction of complementary circuits requires both *n*- and *p*-type unipolar FETs. However, most of TMD semiconductors (MoS_2, WS_2, *etc*.) exhibit n-type characteristics, because dichalcogenides vacancies act as *n*-type dopant.[21-28] Even for tungsten diselenide (WSe_2) with balanced conduction and valence band edges, it usually exhibits ambipolar transport characteristics.[3, 8, 19, 29] Thus, it is of great importance to fabricate unipolar p-type TMD semiconductors FETs to achieve CMOS NC-FETs in a controllable manner.

In this work, we employ different 2D semiconductors (WSe_2 and MoS_2) as channel materials and heterogeneously integrate them onto NC gate stack to form a low-power complementary inverter. The NC gate stack amplifies the gate voltage and reduces the power consumption of the inverter. To enable the formation of unipolar *p*-type FET, we construct vdWs contact by transferring Pt

electrode onto WSe_2 to reduce the gap state at the metal/WSe_2 junction. With highly efficient NC gate stack, the steep slope p-type WSe_2 NC-FET presents a minimal SS of 18 mV/dec. Compared with the 2D semiconductor inverter on silicon oxide, the power consumption of NC inverter is reduced from 1657 pW to 68 pW.

2. Results and Discussion

2.1 2D semiconductor NCFET

Figure 1a is the schematic view of a 2D semiconductor NCFET device, which consists of WSe_2 as the channel (~10 nm thickness), 4 nm Al_2O_3 and 20 nm HZO as the gate dielectric and heavily doped silicon substrate as the gate electrode. A rapid thermal annealing (RTA) in nitrogen ambient was performed at 450 °C for 1.5 min. **Figure 1b** is a scanning transmission electron microscopy (STEM) image taken by a high-angle annular dark-field (HAADF) detector, with a high-resolution STEM (HR-STEM) image of the HZO lattice shown in the inset. Cross-sectional HR-STEM image clearly reveals that the HZO layer is poly-crystalline after the RTA,[30] composed of large HZO grains with high crystal quality. The corresponding elemental maps are shown in **Figure S1**, indicating clear element distribution of the WSe_2, HZO and the Al_2O_3. **Figure 1c** is the polarization versus electric field hysteresis loop (measured at 1 kHZ) of a ferroelectric MIS (Au/HZO/Si) capacitor. We can observe anticlockwise P-E loop, clearly showing ferroelectricity.

Figure 1d shows the transfer characteristics of the WSe_2 NCFET with evaporated Pt electrode on the Al_2O_3/HZO with V_{ds} = -0.1 and -0.5 V, respectively, exhibiting an

ambipolar transport behavior. The *p*-branch current is about 2~3 orders of magnitude larger than that of the *n*-branch. For a CMOS logic unit, the *n*-branch will result in high static current and increase power consumption.[23] SS is extracted for both sweep direction of forward sweep ($SS_{Forward}$) and reverse sweep ($SS_{Reverse}$). The minimum of the $SS_{Reverse}$ is 27 mV/dec and the $SS_{Forward}$ is 88 mV/dec. The corresponding SS versus I_d is given in **Figure 1e**. Although we used NC gate stack in the device, the SS is higher than the thermal limits in higher current range. The ambipolar behavior indicates a large Schottky barrier for both electrons and holes which will degrade electrostatic gate control and decrease the SS and the ON-state current.[1, 31, 32] **Figure 1f** shows the output characteristics of the WSe_2 NC-FET with V_{gs} from -2.5 V to 0 V. The highest current density is 1.7 μA/μm and the output current is nonlinear at small V_{ds}, indicating the presence of energy barrier at the Pt/WSe_2 interface. The ambipolar transport behavior also indicates that the contact between the Pt and the WSe_2 is not Ohmic.[22-24] The Schottky barrier exists at the junction between Pt and the WSe_2, which decreases the ON-state current, and significantly affects the efficient carrier injection from the source electrode.[1, 31, 33] It is very difficult to avoid defects, residues and strain during the conventional fabrication processes. The interface dipoles and metal-induced gap state caused by the defects lead to the Fermi level pinning and result in high Schottky barrier and contact resistance.[5, 34] The ambipolar characteristics prevent the implementation of low-power complementary circuits.

2.2 Unipolar *p*-type WSe_2 NCFET with vdWs contact

To build complementary NCFET inverter, it requires unipolar *n*- and *p*-type NCFETs. The unipolar *n*-type NCFET has been readily realized with typical 2D TMDs in our previous studies.[30] Here we adopt a vdWs contact strategy to realize unipolar *p*-type TMD FETs by reducing the disorder at the contact region, which normally results in Fermi level pinning close to the conduction bond of TMD semiconductors.[23] Unlike three-dimensional covalent semiconductor surface with rich surface dangling bonds and surface reconstructions, the vdWs contact can reduce the dangling band and eliminate the Schockley-Tamm states[4, 5, 24]. The reduction of defects at the metal/WSe_2 interface can shift the Fermi level to the intrinsic position and close to the valence band of WSe_2, making this method promising for constructing *p*-type WSe_2 transistors. By minimizing defects at the Pt/WSe_2 interface, it is reasonable for us to expect a low Schottky barrier height for hole injection. The dangling-bond-free surface avoids the associated chemical disorder and the gap states induced by defects, making it a promising method for fabricating 2D electronic devices.[4, 5] The TEM image of the interface of this vdWs Pt/WSe_2 junction can be seen in **Figure S2**. It is atomically sharp without any defects, disorder and metal diffusion. No damages are observed in the WSe_2 flake under the Pt electrode, indicating that the transfer process is a mild and low-energy fabrication method.

For the SB FETs, the current in the sub-threshold region mainly depends on the thermionic emission current and the thermally-assisted tunneling current. [11, 25-29] When the back-gate voltage (V_g) is below the flat-band voltage (V_{FB}), the thermionic emission current dominates the drain current. The thermionic emission current can be described

according to Equation (1):

$$I_d = AT^{3/2} \exp\left(\frac{q\varphi_B}{k_B T}\right)[1 - \exp(-\frac{qV_{ds}}{k_B T})] \qquad [1]$$

where A^*_{2d} is the 2D equivalent Richardson constant, I_d is the current through the device, T is the absolute temperature, k_B is the Boltzmann constant, q is the unity electron charge, and V_{ds} is the drain to source bias. When V_g is larger than V_{FB}, thermally assisted tunneling current becomes significant, which is not included in the thermal emission theory and results in less effective gate control. When V_g equals to the V_{FB}, the SB height φ_B can be extracted from the slope of $ln\ (I_d/T^{3/2})$ against $1000/T$ since thermally assisted tunneling does not contribute to the current. **Figure 2a** shows the temperature-dependent transfer curve of the WSe_2 FET on SiO_2 with evaporated Pt and transferred Pt electrode at V_{ds} = -0.1 V, respectively. The ON-state current of the WSe_2 FET with transferred Pt electrode is 5 times larger than that with the evaporated Pt electrode. **Figure 2b** presents the Arrhenius plot of the devices with evaporated Pt and transferred Pt electrode and we can calculate the barrier height for different gate voltage from the slope. **Figure 2c** shows the effective SB height as a function of gate voltage for the devices with evaporated Pt and transferred Pt electrode. Obviously, the device with evaporated Pt shows a much higher SB height of 125.8 meV; while the one with the vdWs Pt exhibits a SB of 55.5 meV. The much lower SB height of the device with vdWs contact indicates a better interface at the Pt/WSe_2 junction. The two-terminal temperature-dependent mobility is given in **Figure S3**. The vdWs FET shows a much higher low-temperature mobility compared with the evaporated ones. The small barrier at the transferred Pt/WSe_2 interface reduces the contact resistance and increases the low

temperature mobility.[32] **Figure S4** shows the transfer characteristics of WSe_2 devices on ZrO_2 with evaporated Pt and transferred Pt electrode, in which the transition from ambipolar to unipolar *p*-type is consistent with the device on HZO/Al_2O_3 NC gate stack, clearly demonstrating the effect of contact on the carrier type of a FET. The simplified band diagram is given in **Figure S5a**. The subthreshold swing is defined as $SS = \frac{\partial V_g}{\partial \varphi_s}\frac{\partial \varphi_s}{\partial (log_{10} I_d)} = m \times n$, where V_g is the gate voltage, φ_s is the surface potential of the semiconducting channel, and I_d is the drain current of the transistor.[3, 15, 16] The first item (body factor, *m*), $\frac{\partial V_g}{\partial \varphi_s}$, is determined by the device structure, and the second item (transport factor, *n*), $\frac{\partial \varphi_s}{\partial (log_{10} I_d)}$, is related to the transport mechanism. The contact affects the transport mechanism, and the gate stack influences the surface potential efficiency. The influence of the contact to SS is schematically illustrated in **Figure S5b-c**. With reduced SB barrier, the thermionic region with small SS is broadened, which enables us to get a higher current and efficient control over large gate voltage range.

Figure 2d is the transfer characteristics of the WSe_2 NCFET with transferred Pt electrode. The device exhibits minimum forward $SS_{forward}$ = 44 mV/dec and reverse $SS_{reverse}$ = 18 mV/dec. For the WSe_2 devices with transferred Pt electrode, the *n*-type current was suppressed from nano-amp to pico-amp, exhibiting unipolar *p*-type characteristics. The average SS in the sub-threshold voltage is 47 mV/dec. The drain current can be modulated by 5×10^4 within 220 mV, which is among the smallest among the NCFETs in existing literature, especially for *p*-type FETs. The transfer characteristics with different V_{ds} are given in **Figure S6** and drain induced barrier

lowing of 200 mV/V is observed. **Table S1** shows the comparison of this work with the NCFET devices in the existing literature.[3, 30-32] Our devices show highly efficient gate control over a large current range, indicating the importance of contact in NCFETs. **Figure 2f** is the output characteristics of the NCFET with the highest current of 5.4 μA/μm, which is about 3 times of magnitude larger than that with the evaporated Pt electrode. The output characteristic is linear in the low V_{ds} region and shows good saturation at high V_{ds}.

2.3 Low-power Complementary Inverter with 2D Semiconductor NCFETs

To achieve a complementary circuit, we choose MoS_2 as the *n*-type semiconducting channel material. **Figure 3a-b** show top-view and cross-sectional schematic illustration of the complementary inverter with 2D semiconductor NCFETs. The NC gate stack acts as an amplifier to enhance the gate control, which enables a steeper SS beyond the thermal limits. **Figure 3c** presents the schematic process flow. WSe_2 flakes were mechanically exfoliated onto an Al_2O_3/HZO NC gate stack. Pt electrodes were first fabricated onto a Si substrate, picked up with PVA/PDMS stamp, and aligned onto the WSe_2 flake. The PVA film was washed away and the WSe_2 NC-FET was fabricated (**Figure 3c**(I)). Secondly, MoS_2 flake was exfoliated onto a SiO_2 substrate and then picked with a PVA/PDMS stamp with an Au electrode (**Figure 3c**(II)). Finally, the Au/MoS_2 FET was transferred on the side of the WSe_2 NC-FET. After the PVA being washed away, the complementary NC inverter was fabricated (**Figure 3c**(III)). **Figure 1d** shows an optical image of the WSe_2/MoS_2 NC inverter. The Pt/Au and the Au electrode are marked with different false color.

We also investigate the influence of the transfer process on the device performance. **Figure 4a** is the transfer characteristics of the MoS_2 FET on SiO_2 substrate before and after the transfer process. The MoS_2 FET shows n-type behavior before and after the transfer process. After the transfer process, the V_{th} shifts to the positive side by approximately 11 V, and the current shows degradation. The mobility before and after the transfer process are given in **Figure S6**. The mobility shows little change after the transfer process. The output characteristics are given in **figure 4b**. After the transfer process, the output current decrease from 19 μA/μm to 11 μA/μm. Considering the almost unchanged mobility, the damage caused in the transfer process is acceptable.

The steep slope complementary WSe_2 and MoS_2 NC inverter were fabricated using this stamp method. **Figure 4c** and **Figure 4d** are the representative transfer characteristics of the individual MoS_2 and WSe_2 NCFET, respectively. Both devices show the SS below the thermal limits of 60 mV/dec. For TMD materials, the contact electrodes will influence the threshold voltage of the FET. **Figure 4e** and **Figure 4f** are the output characteristics curve of the individual MoS_2 and WSe_2 NCFET, respectively. The MoS_2 device shows a nonlinear behavior at small V_{ds}, indicating the existence of Schottky barrier at the MoS_2/Au interface. The WSe_2 device shows a linear behavior at small V_{ds}, and starts to saturate at V_{ds} = -1 V.

During the measurement, V_{in} was swept from -3 V to 0 V to switch the inverter. **Figure 5a** shows the voltage transfer curve of the MoS_2-WSe_2 NC-FET inverter under different V_{dd} conditions. As the V_{dd} increases, the threshold voltage shifts to the positive direction. To characterize the robustness of the inverter, we have extracted the

switching threshold and noise margin to V_{dd} as a function of V_{dd}, as shown in **Figure 5b.** As the V_{dd} increases, the threshold voltage shifts to the positive direction. When V_{dd} is higher than 2.0 V, the noise margin is higher than 0.9. **Figure 5c** is the voltage gain obtained from the voltage transfer curve of the inverter. The max gain is 11.7 when the V_{dd} is 2.0 V. A gain larger than 1 is important for cascade logic application because it makes the circuit regenerative and robust to errors.[17] **Figure 5d** is the static current of the inverter from the V_{dd} to the ground. When the V_{dd} is 0.5 V, we get the highest I_{dd} current of 127 pA. The position of the highest current moves to the negative side as the V_{dd} increase. The static power consumption is one of the key factors for low power electronics. **Figure 5e** and **5f** are the static power consumption of the complementary WSe_2/MoS_2 inverter on NC gate stack and SiO_2, respectively. The NCFET inverter shows a maximum gain of 11.7 with ultralow static power consumption of only 68 pW under different V_{dd} from 0.5 V to 2 V, which is one of the lowest power consumptions compared with previous work. [19, 20, 23] While for inverter on SiO_2, the power consumption is about 1657 pW. The low gain is caused by the small capacitance of the 300 nm SiO_2. The performance of WSe_2/MoS_2 CMOS inverter with SiO_2 substrate is given in **Figure S8**.

Conclusion

In summary, we fabricate a pico-watt complementary inverter using 2D semiconductor NCFETs. The vdWs contact changes the ambipolar WSe_2 FET to unipolar *p*-type transistors. More importantly, we reveal the significant role of the SB in reducing the subthreshold slope of WSe_2 FETs. With reduced SB, the thermal region

with steeper SS is widened, the subthreshold current can be modulated over large voltage range, and the saturation current currents show significantly improvement of 5 time. With HZO/Al_2O_3 negative capacitance gate stack, the devices exhibit steep switching characteristics as small as 18 mV/dec, and can be modulated by 5×10^4 within 220 mV, the best one among the *p*-type NCFETs in existing literature. The complementary inverter with 2D semiconductors shows maximum gain of 11.7 with ultra-low power consumption of 68 pW. This method can be used as an effective strategy for low-power electronics by combining with 2D materials and negative capacitance gate stack.

Supporting information

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Method

Device fabrication and electrical measurement

30-nm-thick Pt electrodes were pre-fabricated on a Si substrate using standard photolithography and electron-beam deposition. Transfer method was applied to fabricate the van der Waals contact to 2D materials. Polyvinyl alcohol (PVA) film was used to mechanically pick up the electrodes from the Si substrate. Then the PVA film was attached to a polydimethylsiloxane (PDMS) stamp together with the electrode.

The PVA films was prepared by drying 4% PVA aqueous solution on a CD for 2 days. The temperature during the picking up process was set to be 55 °C for 3 minutes to avoid strong interaction between the electrode and the Si substrate. High drying temperature will result in strong interaction between the PVA film and the Si substrate, which will lead to low yield rate. The back side of the PDMS stamp was attached to a glass slide. 2D WSe_2 flakes were mechanically exfoliated onto top of highly doped Si wafer with 300-nm-thick SiO_2 as the gate dielectric. After we aligned the electrode and the WSe_2 flakes using a 2D materials transfer platform, the PVA thin film with electrodes was physically contacted to the WSe_2 flake. After the alignment, the heat temperature in the contact process was set to be 55 °C for 3 minutes. Finally, the PVA film was washed away with deionization water and isopropanol. Then we transfer an Au electrode first and align the Au electrode to a MoS_2 flake on a SiO_2 substrate. Lift-up the Au/MoS_2 and align the device to the WSe_2 FET. Then heat the device at 55 °C for 3 minutes and wash away the PVA films. All the transfer processes were conducted in ambient environment. Electrical characteristics of fabricated FETs was measured with the Lake Shore TTPX Probe Station and Keithley 4200 SCS under 10^{-5} bar.

ALD deposition

Atom layer deposition (ALD) was used to deposit HZO film on p++ silicon at 180 °C. We use tetrakis (dimethylamido) hafnium as Hf source, tetrakis (dimethylamido) zirconium as Zr source, and H_2O as oxidant. The HfO_2/ZrO_2

ratio was controlled to be 1:1. For capacitance matching and gate leakage reduction, in-situ growth of 4 nm Al_2O_3 was deposited by ALD using trimethylaluminium as Al source and H_2O as oxidant. A rapid thermal annealing in nitrogen environment was performed under 450 °C for 1.5 min to crystallize the HZO and enhance the ferroelectricity.

Cross-sectional TEM sample preparation and characterization

A MultiBeam SEM-FIB system (JIB-4501, JEOL) was used for the cross-sectional sample preparation, operated using 30 keV Ga^+. STEM characterization was performed on a JEOL JEM-2100F TEM/STEM operated at 200 kV, equipped with an Oxford INCA EDS detector and a Gatan Enfina EELS spectrometer for elemental mapping. EELS spectrum imaging was conducted in STEM mode with a 13 mrad convergence angle. The HR-STEM image was acquired from an aberration-corrected JEM-ARM200CF TEM/STEM.

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Figures

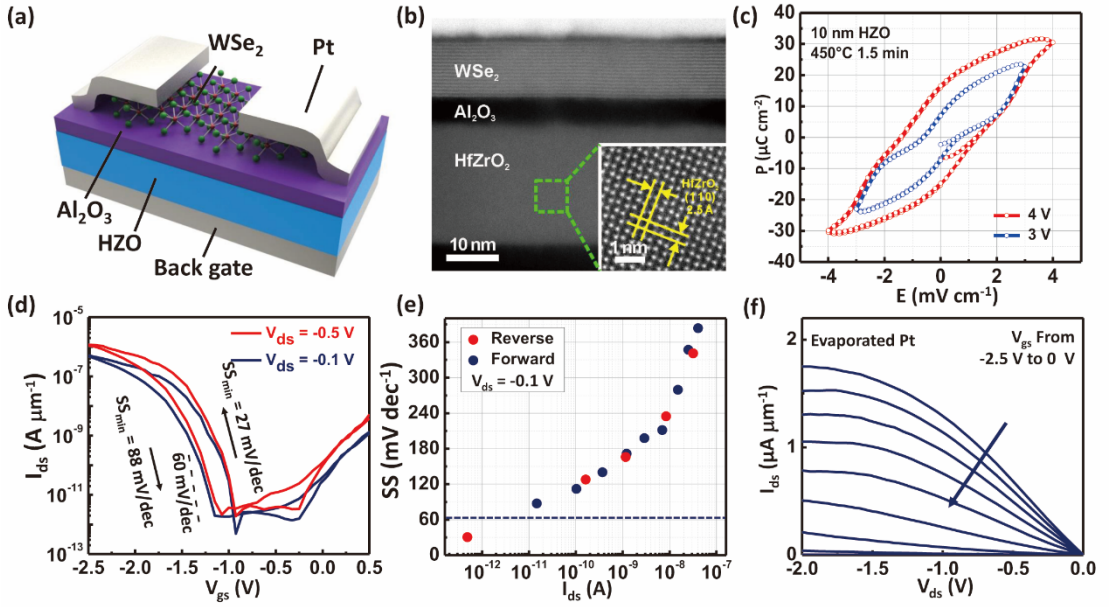

Figure 1. (a) Schematic illustration of a WSe_2 NCFET. (b) HAADF-STEM image of the WSe_2 NCFET. The Scale bar is 10 nm. Inset is the TEM image of HZO. The scale bar is 1 nm. (c) PE loop of the HZO stack. (d) Transfer characteristics of the WSe_2 NCFET with evaporated Pt electrode. The channel length is 5 μm. (e) Subthreshold slope of the WSe_2 NCFET with evaporated Pt electrode. (f) Output characteristics of the WSe_2 NCFET with evaporated Pt electrode.

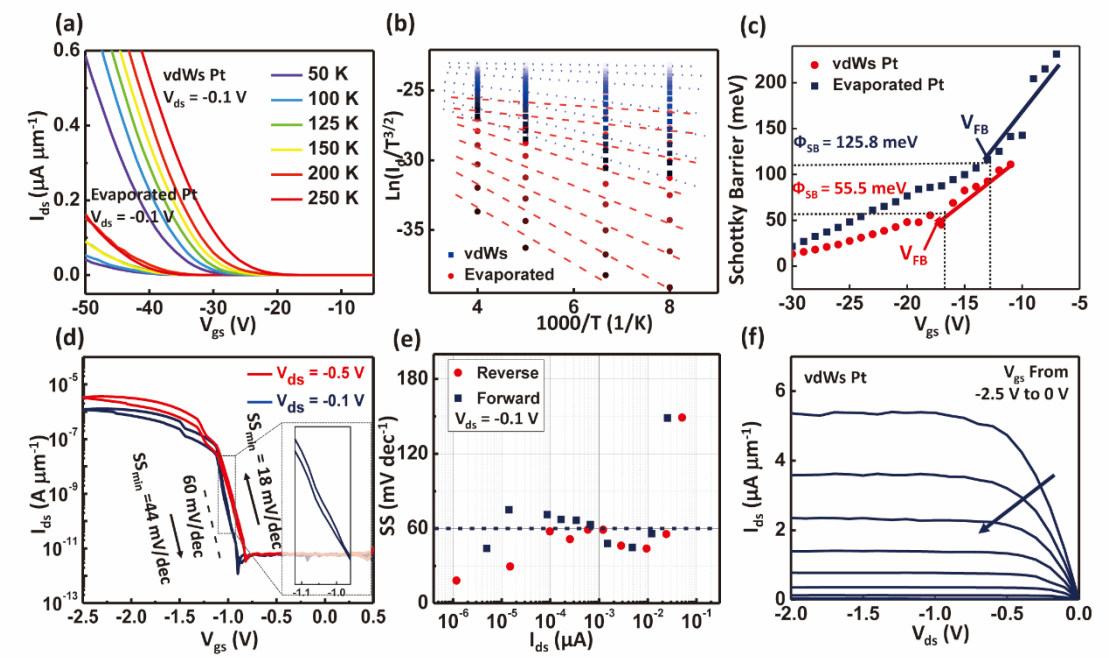

Figure 2. (a) Temperature dependent transfer curve of the FET with evaporated Pt and transferred Pt electrode on 300 nm SiO_2. The channel length is 5 μm. (b) Arrhenius plot of the temperature dependent current. (c) Schottky barrier height of the $Pt_{evaporated}/WSe_2$ junction. (d) Transfer characteristics of the WSe_2 NCFET with transferred Pt electrode. The channel length is 5 μm. (e) Subthreshold slope of the WSe_2 NCFET with transferred Pt electrode. (f) Output characteristics of the WSe_2 NCFET with transferred Pt electrode.

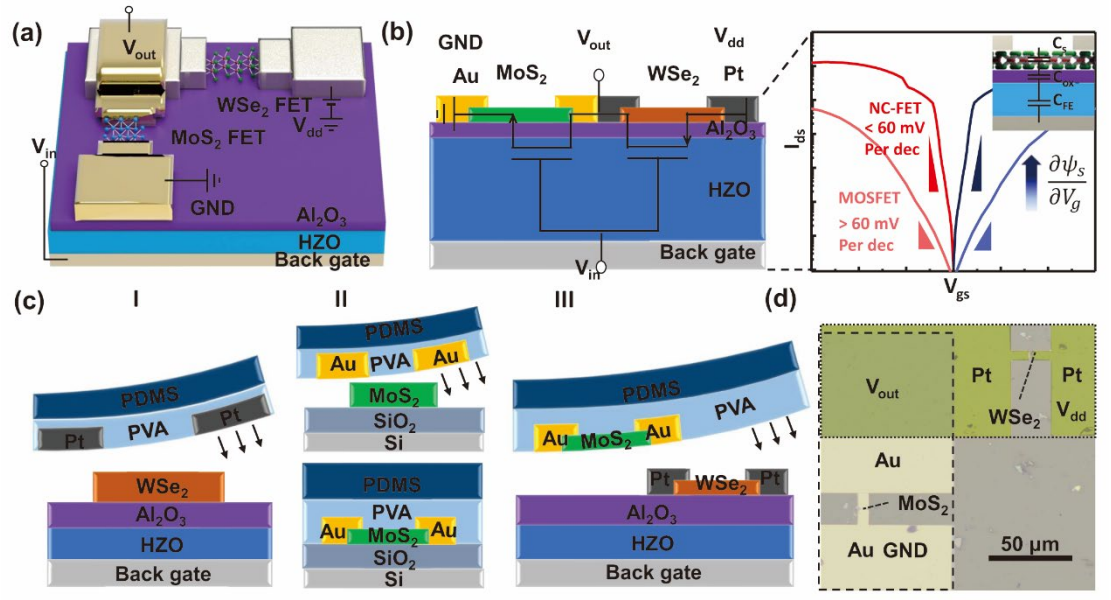

Figure 3. (a) Schematic illusion of a WSe_2/MoS_2 NCFET inverter. (b) Side view schematic illusion of the WSe_2/MoS_2 negative capacitance inverter. (c) Fabrication process of the complementary inverter. (d) Optical image of the WSe_2/MoS_2 negative capacitance inverter. The Au and Pt electrode of the MoS_2 and WSe_2 transistor are connected to the GND and V_{dd} power supply. The Si gate serves as the input node and the cross point of the electrode is used as output node. The electrode is marked with different color. the scale bar is 50 μm.

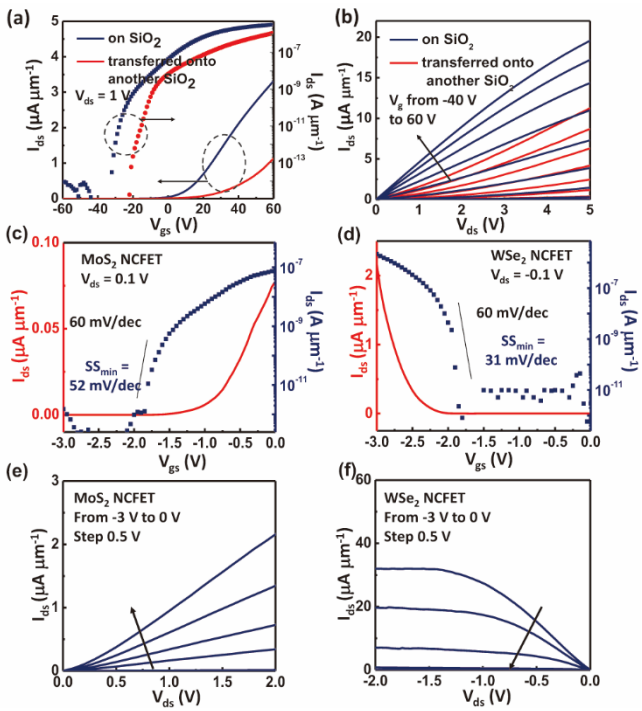

Figure 4. (a) Transfer curves of MoS_2 FETs on SiO_2 with transferred Au contact before and after the transfer process. The channel length is 5 μm. (b) Output curves of MoS_2 FETs on SiO_2 before and after the transfer process. (c) Transfer characteristics of the MoS_2 *n*-type NCFET with Au electrode. The channel length is 5 μm. (d) Transfer characteristics of the WSe_2 *p*-type NC-FET with transferred Pt electrode. (e-f) Output characteristics of the MoS_2 and WSe_2NCFETs.

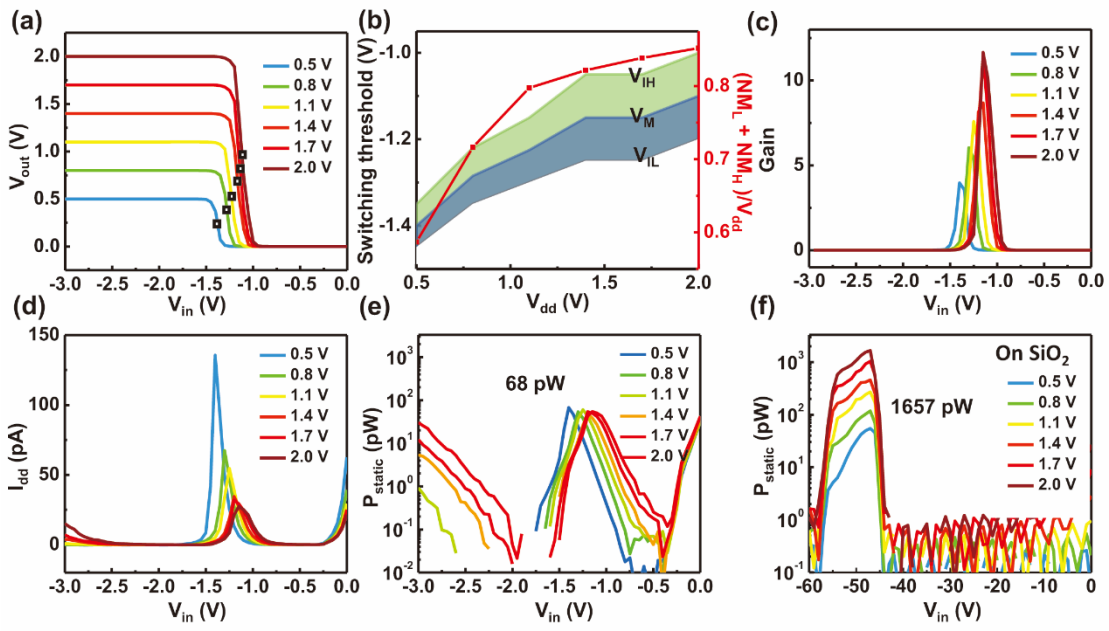

Figure 5. (a) Voltage transfer of the WSe_2/MoS_2 NCFET inverter as a function of input voltage. (b) Switching threshold and noise margin to V_{dd} as a function of V_{dd}. (c)Voltage gain as a function of input voltage. (d) Static current from the power supply to the ground. (e) Static power consumption of the WSe_2/MoS_2 negative capacitance inverter during the scanning process of the input voltage. (f) Static power consumption of the WSe_2/MoS_2 inverter on SiO_2.